



U74LVC16244

Advance

CMOS IC

16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

DESCRIPTION

This 16-bit buffer/driver is designed for 1.65V to 3.6V V_{CC} operation.

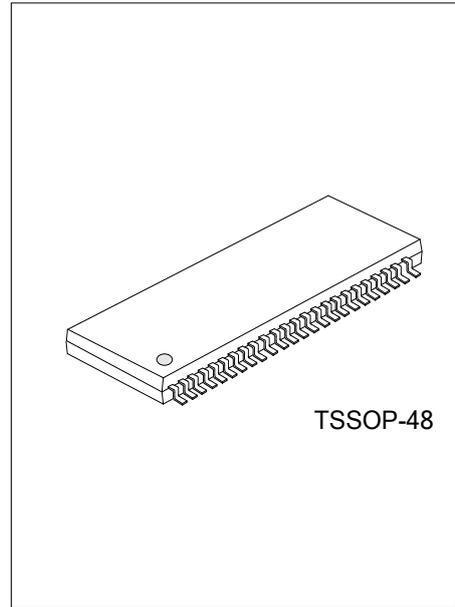
The **U74LVC16244A** is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V system environment.

This device is fully specified for partial-power-down applications using I_{OFF} . The I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



TSSOP-48

FEATURES

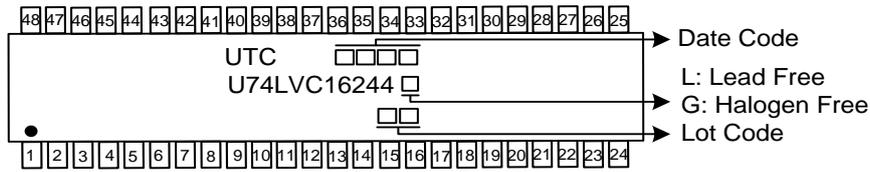
- * Wide supply voltage range from 1.65V to 3.6V
- * Inputs accept voltages up to 5.5V
- * I_{OFF} supports partial-power-down mode
- * Low static power consumption; $I_{CC}=10\mu A$ (Max.)

ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC16244L-P48-R	U74LVC16244G-P48-R	TSSOP-48	Tape Reel

<p>U74LVC16244G-P48-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) P48: TSSOP-48</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



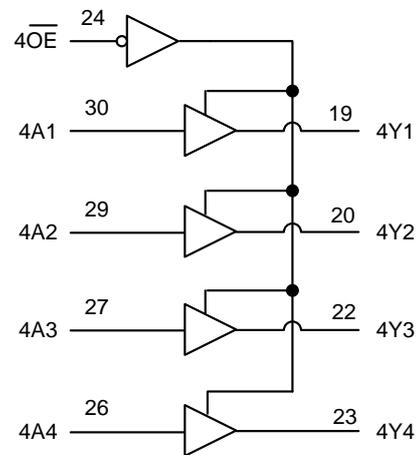
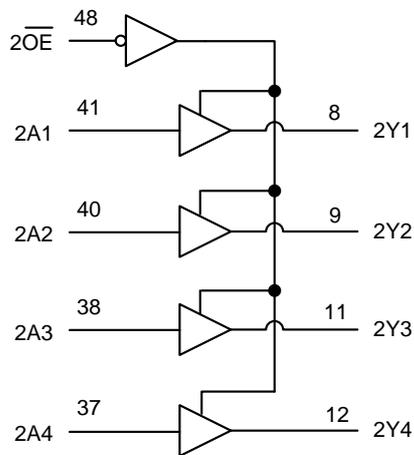
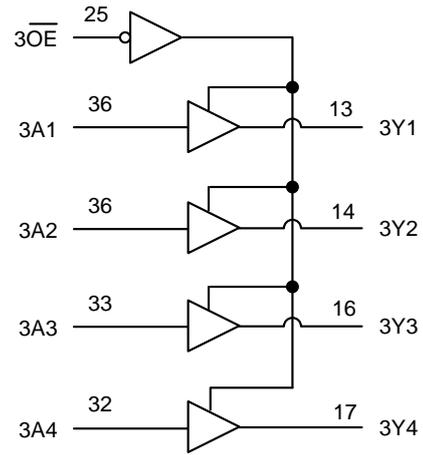
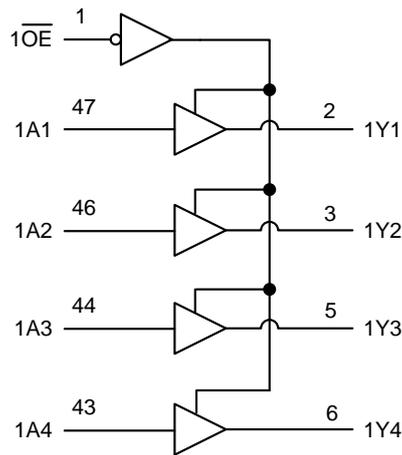
PIN CONFIGURATION



■ **FUNCTION TABLE** (each gate)

INPUT(\overline{OE})	INPUT(A)	OUTPUT(Y)
L	H	H
L	L	L
H	X	Z

■ **LOGIC DIAGRAM** (Positive Logic)



■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C , unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V _{CC}		-0.5 ~ 6.5	V
Input Voltage	V _{IN}		-0.5 ~ 6.5	V
Output Voltage	V _{OUT}	Output in high-impedance or power-off state	-0.5 ~ 6.5	V
		Output in high or low state	-0.5 ~ V _{CC} +0.5	V
Input Clamp Current	I _{IK}	V _I <0	-50	mA
Output Clamp Current	I _{OK}	V _O <0	-50	mA
Output Current	I _{OUT}		±50	mA
Continuous current through V _{CC} or GND	I _{CC}		±100	mA
Storage Temperature	T _{STG}		-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING CONDITIONS (T_A=25°C , unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V _{CC}	Operating	1.65		3.6	V
		Data Retention Only	1.5			V
Input Voltage	V _{IN}		0		5.5	V
Output Voltage	V _{OUT}	Active state	0		V _{CC}	V
		3-state	0		5.5	
High-Level Input Voltage	V _{IH}	V _{CC} =1.65V~1.95V	0.65×V _{CC}			V
		V _{CC} =2.3V~2.7V	1.7			V
		V _{CC} =2.7V~3.6V	2			V
Low-Level Input Voltage	V _{IL}	V _{CC} =1.65V~1.95V			0.35×V _{CC}	V
		V _{CC} =2.3V~2.7V			0.7	V
		V _{CC} =2.7V~3.6V			0.8	V
Operating Temperature (Note)	T _A		-40		+125	°C
Input Transition Rise or Fall Rate	Δt/Δv				10	ns/V

■ ELECTRICAL CHARACTERISTICS (T_A=25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Output Voltage	V _{OH}	V _{CC} =1.65V~3.6V, I _{OH} =-100uA	V _{CC} -0.2			V
		V _{CC} =1.65V, I _{OH} =-4mA	1.2			V
		V _{CC} =2.3V, I _{OH} =-8mA	1.7			V
		V _{CC} =2.7V, I _{OH} =-12mA	2.2			V
		V _{CC} =3V, I _{OH} =-12mA	2.4			V
		V _{CC} =3V, I _{OH} =-24mA	2.2			V
Low-Level Output Voltage	V _{OL}	V _{CC} =1.65V~3.6V, I _{OL} =100uA			0.2	V
		V _{CC} =1.65V, I _{OL} =4mA			0.45	V
		V _{CC} =2.3V, I _{OL} =8mA			0.7	V
		V _{CC} =2.7V, I _{OL} =12mA			0.4	V
		V _{CC} =3V, I _{OL} =24mA			0.55	V
Input Leakage Current (A and \overline{OE} Inputs)	I _{I(LEAK)}	V _{CC} =3.6V, V _{IN} =0~5.5V			±5	μA
Power OFF Leakage Current	I _{OFF}	V _{CC} =0V, V _{IN} or V _{OUT} =5.5V			±10	μA
Output OFF-State Current	I _{OZ}	V _{CC} =3.6V, V _{OUT} =0 or 5.5V			±10	μA
Quiescent Supply Current	I _{CC}	V _{CC} = 3.6V, V _{IN} =V _{CC} or GND, I _{OUT} =0A			20	μA
		V _{CC} = 3.6V, V _{IN} =3.6V≤V _{IN} ≤5.5V, I _{OUT} =0A (Note 2)			20	μA
Additional Quiescent Supply Current Per Input Pin	ΔI _{CC}	V _{CC} =2.7V~3.6V, One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND			500	μA
Input Capacitance	C _I	V _{CC} =3.3V, V _{IN} =V _{CC} or GND		5.5		pF
Output Capacitance	C _O	V _{CC} =3.3V, V _{OUT} =V _{CC} or GND		6		pF

Notes: 1. All typical values are at V_{CC} = 3.3V, T_A = 25°C.

2. This applies in the disabled state only.

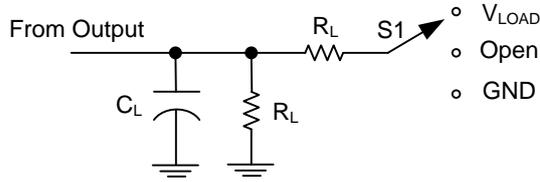
■ SWITCHING CHARACTERISTICS (T_A=25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
From Input(A) to Output(Y)	t _{pd}	V _{CC} =1.8V±1.5V	0.5		6.6	ns
		V _{CC} =2.5V±0.2V	0.5		5.9	ns
		V _{CC} =2.7V	0.5		4.7	ns
		V _{CC} =3.3V±0.3V	0.5		4.1	ns
From Input(\overline{OE}) to Output(Y)	t _{en}	V _{CC} =1.8V±1.5V	0.5		7.5	ns
		V _{CC} =2.5V±0.2V	0.5		6.7	ns
		V _{CC} =2.7V	0.5		5.8	ns
		V _{CC} =3.3V±0.3V	0.5		4.6	ns
From Input(\overline{OE}) to Output(Y)	t _{dis}	V _{CC} =1.8V±1.5V	0.5		10.3	ns
		V _{CC} =2.5V±0.2V	0.5		8.3	ns
		V _{CC} =2.7V	0.5		6.2	ns
		V _{CC} =3.3V±0.3V	0.5		5.8	ns
Output Skew Time	t _{SK(O)}	V _{CC} =3.3±0.3V			1	ns

■ OPERATING CHARACTERISTICS (f=10MHz, T_A=25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	Outputs Enabled	V _{CC} =1.8V		33		pF
		V _{CC} =2.5V		35		pF
		V _{CC} =3.3V		39		pF
	Outputs Disabled	V _{CC} =1.8V		2		pF
		V _{CC} =2.5V		3		pF
		V _{CC} =3.3V		4		pF

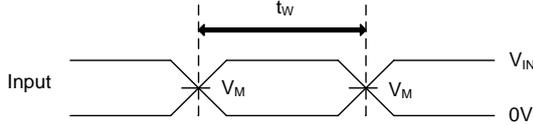
TEST CIRCUIT AND WAVEFORMS



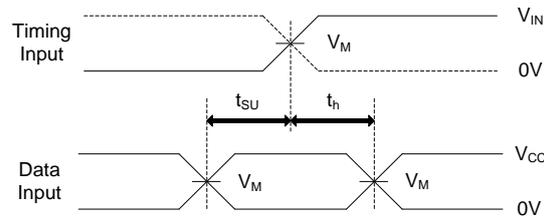
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

TEST CIRCUIT

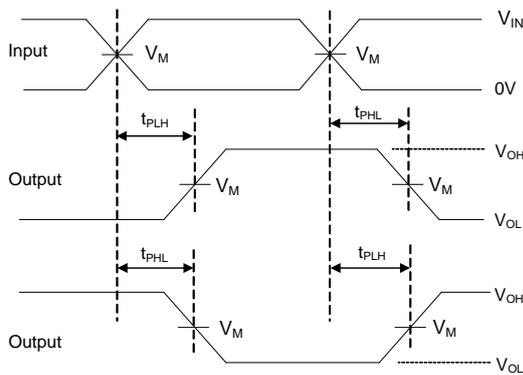
V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_{IN}	t_R, t_F					
$1.8V \pm 0.15V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	30pF	1K Ω	0.15V
$2.5V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	30pF	500 Ω	0.15V
2.7V	2.7V	$\leq 2.5ns$	1.5V	6V	50pF	500 Ω	0.3V
$3.3V \pm 0.3V$	2.7V	$\leq 2.5ns$	1.5V	6V	50pF	500 Ω	0.3V



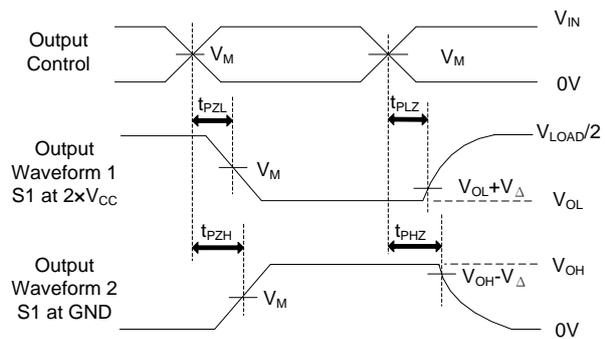
PULSE DURATION



SETUP AND HOLD TIMES



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10MHz$, $Z_O = 50\Omega$.

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