

U74AUP1T34

CMOS IC

1-BIT UNIDIRECTIONAL VOLTAGE-LEVEL TRANSLATOR

■ DESCRIPTION

The **U74AUP1T34** device is a 1-bit noninverting translator that uses two separate configurable power supply rails. It is a uni-directional translator from A to B. The A port is designed to track V_{CCA} . V_{CCA} accepts supply voltages from 0.9V to 3.6V. The B port is designed to track V_{CCY} . V_{CCY} accepts supply voltages from 0.9V to 3.6V. This allows for low-voltage translation between 1V, 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V voltage nodes. The **U74AUP1T34** is also fully specified for partial-power-down applications using I_{OFF} . The I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if V_{CCA} input is at GND, the B port is in the high-impedance state.

■ FEATURES

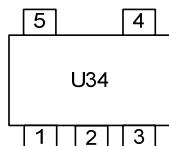
- * Wide supply voltage range from 0.9V to 3.6V
- * Inputs accept voltages up to 3.6V
- * I_{OFF} supports partial-power-down mode
- * Low static power consumption; $I_{CC}=5\ \mu A$ (Max.)

■ ORDERING INFORMATION

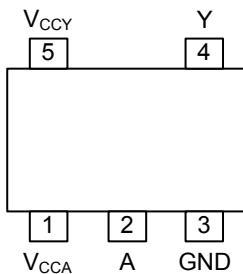
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AUP1T34L-AE5-R	U74AUP1T34G-AE5-R	SOT-23-5	Tape Reel
U74AUP1T34L-AL5-R	U74AUP1T34G-AL5-R	SOT-353	Tape Reel

U74AUP1T34G-AE5-R 	(1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) AE5: SOT-23-5, AL5: SOT-353 (3) G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING



■ PIN CONFIGURATION



■ PIN DESCRIPTION

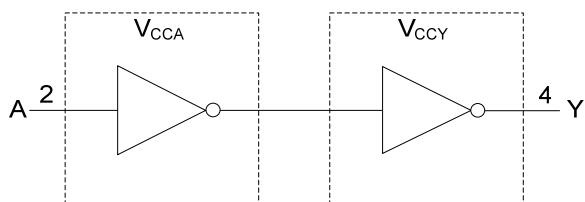
PIN NO.	PIN NAME	I/O	DESCRIPTION
1	V _{CCA}		Input Port DC Power Supply
2	A	I	Input Port
3	GND		Ground
4	Y	O	Output Port
5	V _{CCY}		Output Port DC Power Supply

■ FUNCTION TABLE (each gate)

INPUT	OUTPUT
A PORT	B PORT
L	L
H	H

Note: H: HIGH voltage level; L: LOW voltage level.

■ LOGIC DIAGRAM (positive logic)



■ FEATURE DESCRIPTION

Fully Configurable Dual-Rail Design

Both V_{CCA} and V_{CCY} can be supplied at any voltage from 0.9V to 3.6V, making the device suitable for translating between any of the voltage nodes (1V, 1.2V, 1.8V, 2.5V, and 3.3V).

Partial-Power-Down Mode Operation

I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the **U74AUP1T34** when it is powered down. This can occur in applications where subsections of a system are powered down (partial-powerdown) to reduce power consumption.

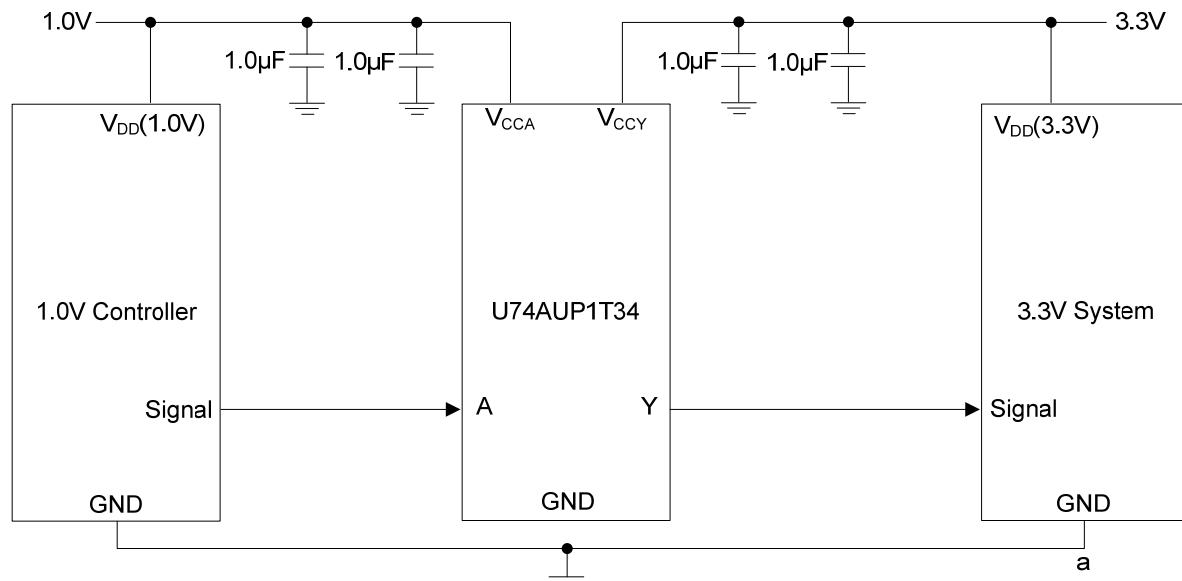
V_{CC} Isolation

The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCY} are at GND (or < 0.4V), both ports A and B are set to a high-impedance state, preventing false logic levels from being presented to either bus.

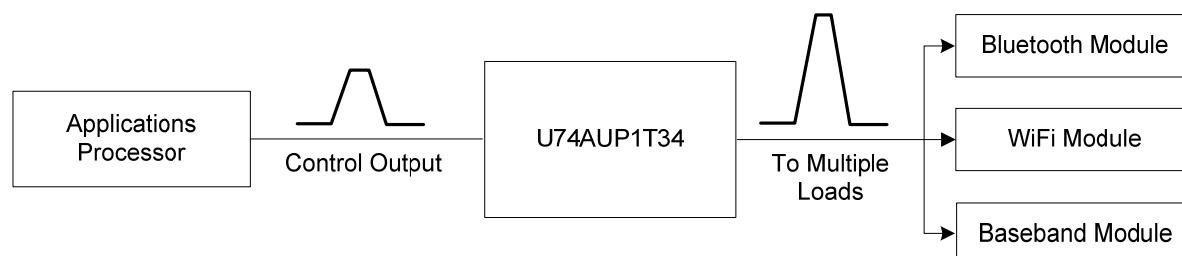
Input Hysteresis

Input hysteresis allows the input to support slew rates as slow as 200ns/V, improving switching noise immunity.

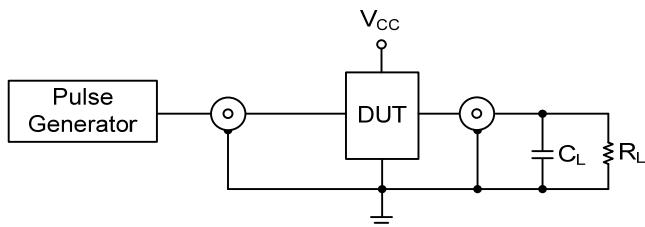
■ TYPICAL APPLICATION



■ EXAMPLE APPLICATION



■ TEST CIRCUIT AND WAVEFORMS



Definitions for test circuit:

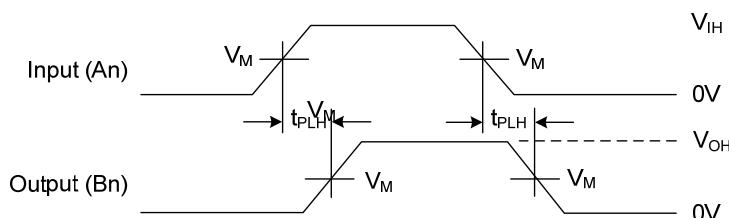
t_{PLH} / t_{PHL}

$C_L = 5\text{pF}, 10\text{pF}, 15\text{pF}, 30\text{pF}$ or equivalent (includes probe and jig capacitance).

$R_L = 1\text{M}\Omega$ or Equivalent.

Z_{OUT} of pulse generator=50 Ω

V_{CCA} / V_{CCY}	V_{IN}	$t_R = t_F$	V_M
1.1V ~ 3.6V	V_{CCA}	$\leq 3.0\text{ns}$	$0.5 \times V_{CCA}$



Notes: 1. $V_{MI}=V_{IH}/2$, $V_{MO}=V_{CCB}/2$

2. $t_R=t_F=2.0\text{ns}$, 10% to 90%, $f=1\text{MHz}$, $t_w=500\text{ns}$

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