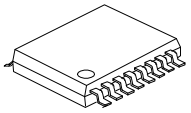
8 CHANNEL SERIAL INTERFACE LOW-SIDE DRIVER



TSSOP-16

■ DESCRIPTION

The **U8C3060** provides an 8-channel low side driver with overcurrent protection and open/shorted load detection. It has built-in diodes to clamp turn-off transients generated by inductive loads, and can be used to drive unipolar stepper motors, DC motors, relays, solenoids, or other loads.

U8C3060 can supply up to 200mA × 8 channel continuous output current. The current driving capability increased with lower PWM duty cycle. A single channel can deliver up to 560 mA continuous output current.

A serial interface is provided to control the **U8C3060** output drivers, configure internal setting register and read the fault status of each channel. Multiple **U8C3060** devices can be daisy-chained together to use a single serial interface. Energizing-time and holding-PWM-Duty cycles are configurable through serial interface as well. These functions allow for cooler running than traditional always-on solutions.

Internal shutdown functions are provided for overcurrent protection, short-circuit protection, under voltage lockout, and overtemperature.**U8C3060** can diagnosis an open load condition. Fault information for each channel can be read out through serial interface and indicated by an external fault pin.

■ FEATURES

* 8 Channel Protected Low-side Driver
  Eight NMOS FETs with Overcurrent Protection
  Integrated Inductive Catch Diodes
  Serial Interface
  Open/Short Load Detection
  Configurable 100% Output Timing
  Configurable PWM Duty Cycle
* Continuous Current Driving Capability
  560 mA (Single Channel)
  200 mA (8 Channels)
  Support Parallel Configuration
* 8 V to 38 V Supply Voltage Range
* Input Digital Noise Filter for Noise Immunity
* Internal Data Read Back Capability for Reliable Control
* Protection and Diagnostic Features
  Overcurrent Protection (OCP)
  Open Load Detection (OL)
  Over Temperature Shutdown (OTS)
  Under Voltage Lockout (UVLO)
  Individual Channel Status Report
  Fault Condition Alarm

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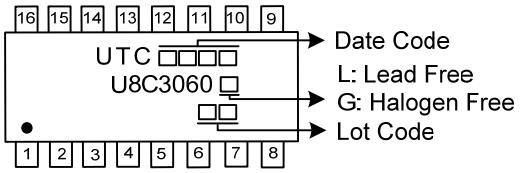
■ ORDERING INFORMATION

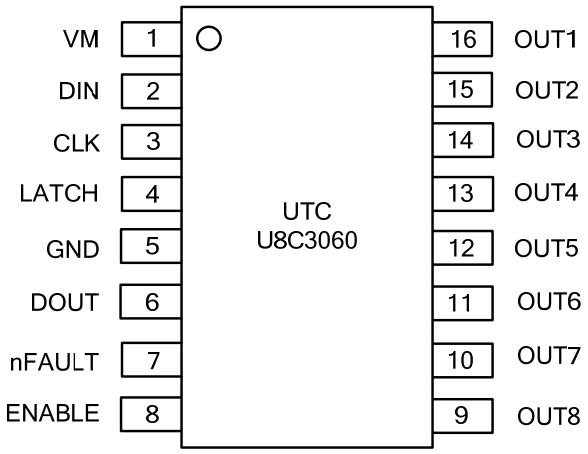
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U8C3060L-P16-R	U8C3060G-P16-R	TSSOP-16	Tape Reel

U8C3060G-P16-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) P16: TSSOP-16 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION



■ PIN DESCRIPTION

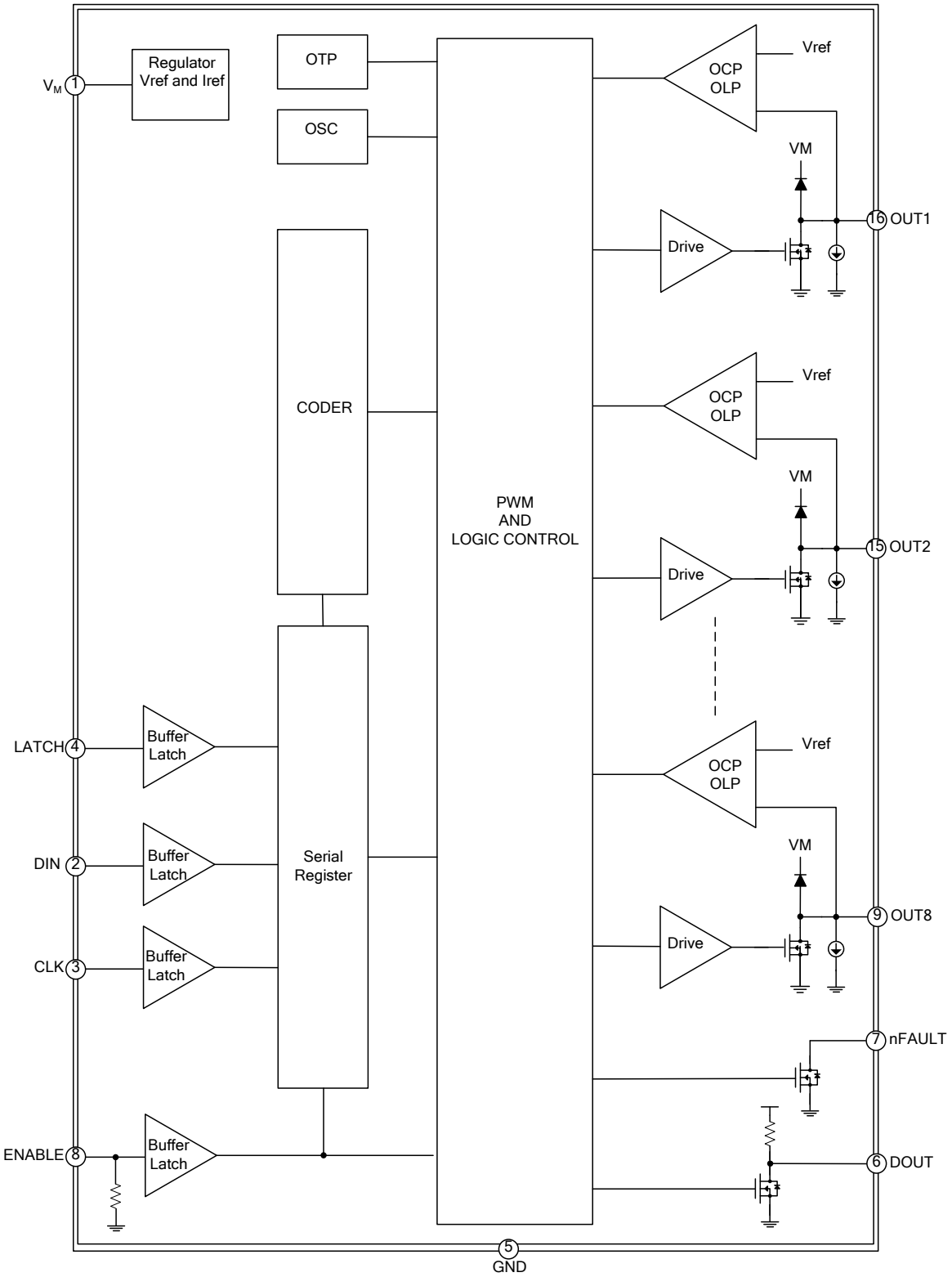
PIN NO.	PIN NAME	DESCRIPTION
1	V_M	Motor power supply
2	DIN	Serial data input; Serial data input from controller. Internal pulldown.
3	CLK	Serial clock input; Rising edge clocks data into part for write operations. Falling edge clocks data out of part for read operations. Internal pulldown.
4	LATCH	Serial latch signal; Refer to serial communication waveforms. Internal pulldown.
5	GND	Device ground
6	DOUT	Serial data output; Serial data output to controller. Open-drain output with internal pullup.
7	nFAULT	Logic low when in fault condition. Open-drain output requires external pullup. Faults: OCP, OL, OTS, UVLO
8	ENABLE	Logic high to enable outputs, logic low to disable outputs. Internal logic and registers can be read and written to when ENABLE is logic low. Internal pulldown.
9	OUT8	NFET output driver. Connect external load between this pin and V_M
10	OUT7	
11	OUT6	
12	OUT5	
13	OUT4	
14	OUT3	
15	OUT2	
16	OUT1	

Table 1. External Components

COMPONENT	PIN1	PIN2	RECOMMENDED
$C_{(VM)}$	V_M	GND	0.1 μF ceramic capacitor rated for V_M
			10 μF electrolytic capacitor rated for V_M
$R_{(nFAULT)}$	V3P3 (Note)	nFAULT	> 4.7 kΩ

Note: V3P3 is not a pin on the **U8C3060**, but a V3P3 supply voltage pullup is required for open-drain output nFAULT.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Power supply voltage range	V_M	-0.3 ~ 40	V
Digital input pin current range	DIN、LATCH、CLK、ENABLE	0 ~ 20	mA
Digital output pin voltage range	nFAULT、DOUT	-0.5 ~ 7	V
Digital output pin current	nFAULT、DOUT	-0.5 ~ 7	V
Output voltage range	OUT_X	-0.3 ~ 40	V
Output current range	OUT_X	Internally limited	A
Operating vitual junction temperature range	T_J	-40 ~ +150	°C
Storage temperature range	T_{STG}	-60 ~ +150	°C

Note：1.Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. All voltage values are with respect to network ground terminal.
3. Power dissipation and thermal limits must be observed.

■ RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Motor power supply voltage range	V_M	8		38	V
Low-side driver current capability	I_{OUT}			560	mA
Operating ambient temperature range	T_A	-40		85	°C

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	103	°C/W

■ ELECTRICAL CHARACTERISTICS

(T_A = 25°C, over recommended operating conditions unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
VM operating supply current	$I_{(VM)}$	V_M=24V		3	4.5	mA
VM under voltage lockout voltage	$V_{(UVLO)}$	V_M rising			8.2	V
LOGIC-LEVEL INPUTS (DIN, ENABLE,CLK,LATCH,)						
Input low voltage	V_{IL}		0		0.7	V
Input high voltage	V_{IH}		1.5		5.3	V
Input hysteresis	V_{HYS}		100			mV
Input low current	V_{IL}	V_{IN}=0	-20		20	uA
Input high current	V_{IH}	V_{IN}=3.3V			100	uA
Input pulldown resistance	R_{PD}			125		kΩ
DOUT,nFAULT OUTPUTS (OPEN-DRAIN OUTPUTS)						
Output low voltage	V_{OL}	I_O=5mA			0.5	V
Output high leakage current	I_{OH}	V_O=3.3V,nFAULT	-1		1	uA
Input pullup resistance	R_{PU}	DOUT only (Pull up to internal 5.7V)		1.4		kΩ
LOW-SIDE FET DRIVERS						
FET on resistance	$R_{DS(ON)}$	V_M=24V,I_O=150mA		3		Ω
Off-state leakage current	I_{OFF}	V_M=24V	0	30		uA
HIGH-SIDE FREE-WHEELING DIODES						
Diode forward voltage	V_F	V_M=24V,I_O=150mA		0.9		V
PROTECTION CIRCUITS						
Overcurrent protection trip level	I_{OCP}	Each channel separately monitored		620		mA
Open load detect pull-down current	I_{OL}	Each channel separately monitored		30		μA
Open load detect threshold voltage	V_{OL}	Each channel separately monitored		1.2		V
Thermal shutdown temperature	T_{TSD}	Die temperature	150	160	180	°C
Thermal shutdown hysteresis	T_{HYS}	Die temperature		35		°C
PWM CHOPPING FREQUENCY						
PWM chopping frequency	F_{PWM}	Duty cycle is >25%		40		kHz
		Duty cycle is 25%		20		
		Duty cycle is 12.5%		10		

■ TIMING REQUIREMENTS

PARMMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Rise time	t_R	I_O=150mA,V_M=24V, resistive load	50		300	ns
Fall time	t_F		50		300	ns
Overcurrent protection deglitch time	t_{OCP}	V_M=24V	2.7	3.5	3.85	μs
Open load detect deglitch time	t_{OL}	Each channel separately monitored	14	17	20	μs

■ SERIAL INTERFACE

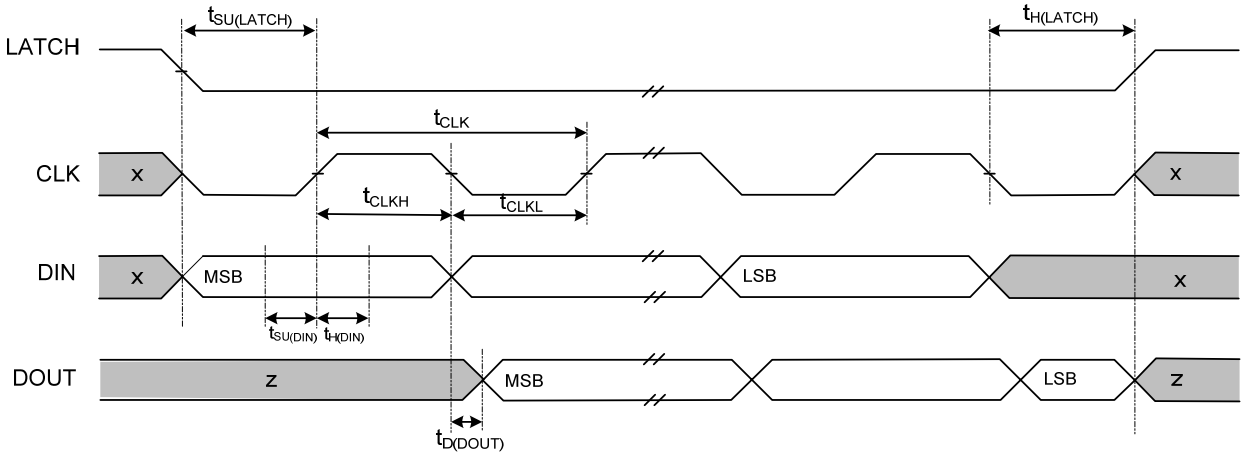


Table 2. Serial Timing

NO.	REF DES	DESCRIPTION	MIN	TYP	MAX	UNIT
1	t_{CLK}	CLK cycle time	5			μs
2	t_{CLKH}	CLK high time	2.5			μs
3	t_{CLKL}	CLK low time	2.5			μs
4	$t_{SU(DIN)}$	Setup time, DIN to CLK	1			μs
5	$t_{H(DIN)}$	Hold time, DIN to CLK	1			μs
6	$t_{SU(LATCH)}$	Setup time, LATCH to CLK	1			μs
7	$t_{H(LATCH)}$	Hold time, LATCH to CLK	1			μs
8	$t_{OFF(LATCH)}$	Inactive time between writes and read	2			μs
9	$t_{D(DOUT)}$	Delay time, CLK to DOUT			1.5	μs

■ SPECIAL COMMANDS

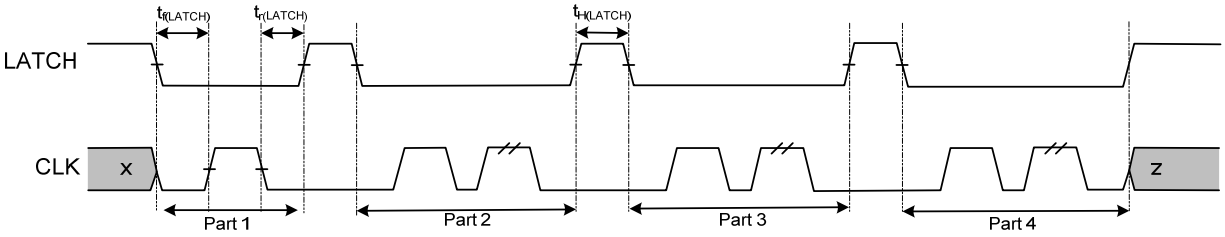


Table 3. Special Commands

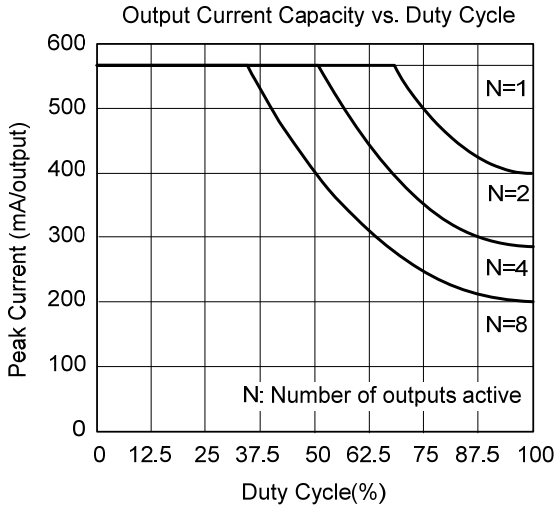
NO.	REF DES	DESCRIPTION	MIN	TYP	MAX	UNIT
10	$t_{f(LATCH)}$	LATCH fall to CLK rise	1			μs
11	$t_{r(LATCH)}$	CLK fall to LATCH rise	1			μs
12	$t_{H(LATCH)}$	LATCH high time	2			μs

■ RECOMMENDED OUTPUT CURRENT

Table 4. OUTPUT CURRENT RECOMMENDATION (T_A = 25°C)

CONFIGURATION	OUTPUT CURRENT CAPACITY
1x output on (100% duty cycle)	566mA
2x outputs on (100% duty cycle)	400mA per output
4x outputs on (100% duty cycle)	283mA per output
8x outputs on (100% duty cycle)	200mA per output

Note: **U8C3060** current capability will depend on several system application parameters such as system ambient temperature, maximum case temperature, and overall output duty cycle.



■ SINGLE DEVICE CONNECTION

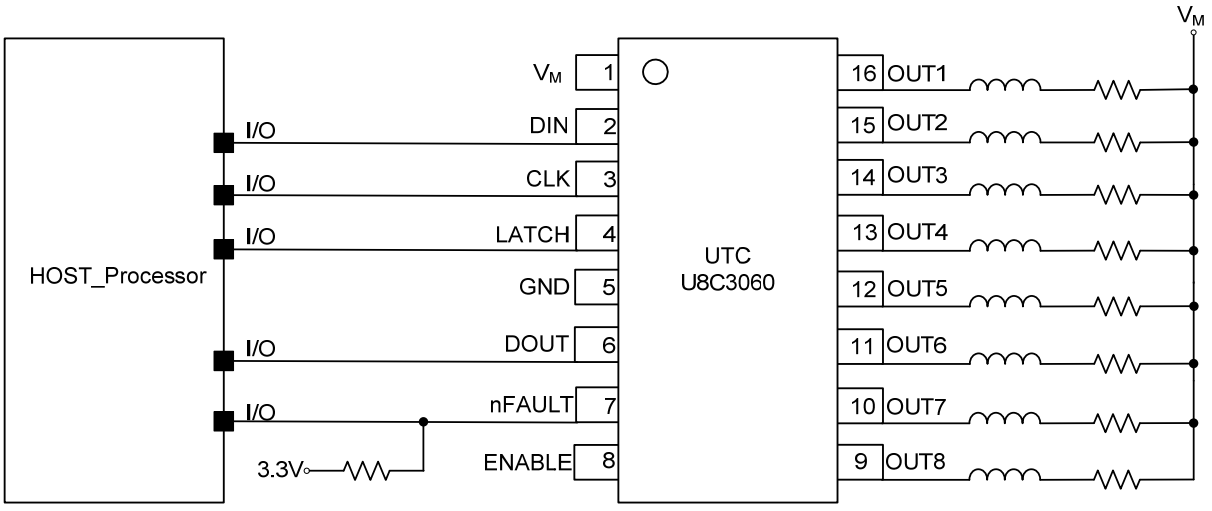


Fig 1. Single Device Connection

■ DAISY-CHAIN CONNECTION

Two or more **U8C3060** devices may be connected together to use a single serial interface. The DOUT pin of the first device in the chain is connected to the DIN pin of the next device. The CLK, LATCH, RESET, and nFAULT pins are connected together.

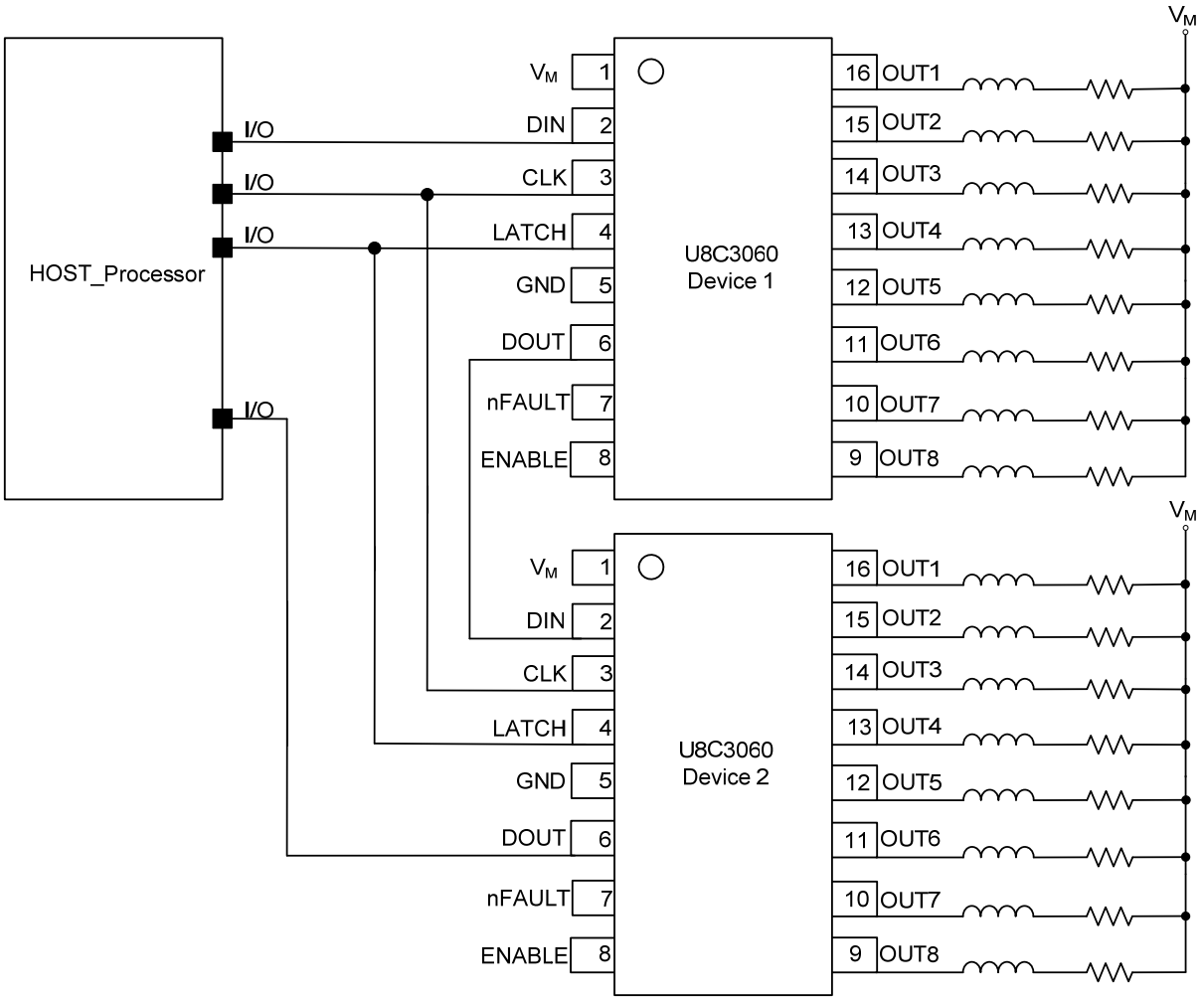


Fig 2. Daisy-Chain Connection

■ REGISTER MAPS

Data Register

The Data register is used to control the status of each of the eight outputs:

Table 5. Data Register

D1	D2	D3	D4	D5	D6	D7	D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7	OUT8

LEGEND: R/W=Read/Write;

When any bitis '1', the corresponding output will be active. When any bitis '0', the output will be inactive.

The data register is the default write location for the serial interface. In order to read back data from this register, the Data Register Readout special command is used.

Fault Register

The Fault register can be read to determine if any channel exist fault condition. OCP is an overcurrent fault and OLD is an open load fault.

Table 6. Fault Register

F1	F2	F3	F4	F5	F6	F7	F8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
OUT1_OL	OUT2_OL	OUT3_OL	OUT4_OL	OUT5_OL	OUT6_OL	OUT7_OL	OUT8_OL
F9	F10	F11	F12	F13	F14	F15	F16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
OUT1_OCP	OUT2_OCP	OUT3_OCP	OUT4_OCP	OUT5_OCP	OUT6_OCP	OUT7_OCP	OUT8_OCP

LEGEND: R/W=Read/Write;

When any fault occurs, nFAULT pin will be driven low and corresponding Fault register bit will be set up as'1'.
OCP is a flag indicating overcurrent fault. ODP is a flag indicating open load fault.
Fault bits can be reset by two approaches:

1. Special command 'FAUL TRESET' clear all fault bits.
2. Setting Data register to ON will clear corresponding OLD bits.

Setting Data register to OFF will clear corresponding OCP bits.

Control Register

The Control register is used to adjust the Energizing Time and PWM Duty Cycle of outputs:

Table 7. Control Register

C1	C2	C3	C4	C5	C6	C7	C8
R/W				R/W			R/W
Energizing Time control				PWM Duty Cycle control			Over All Enable

LEGEND: R/W=Read/Write;

Special command 'WRITE CONTROL REGISTER' is used to program control register.
Special command 'READ CONTROL REGISTER' is used to readback control register content.

■ PROGRAMMING

Serial Control Interface

U8C3060 is using a daisy chain serial interface. Data is latched into the register on the rising edge of the LATCH pin. Data is clocked in on the rising edge of CLK when writing, and data is clocked out on the falling edge of CLK when reading.

Data Writing Wave form

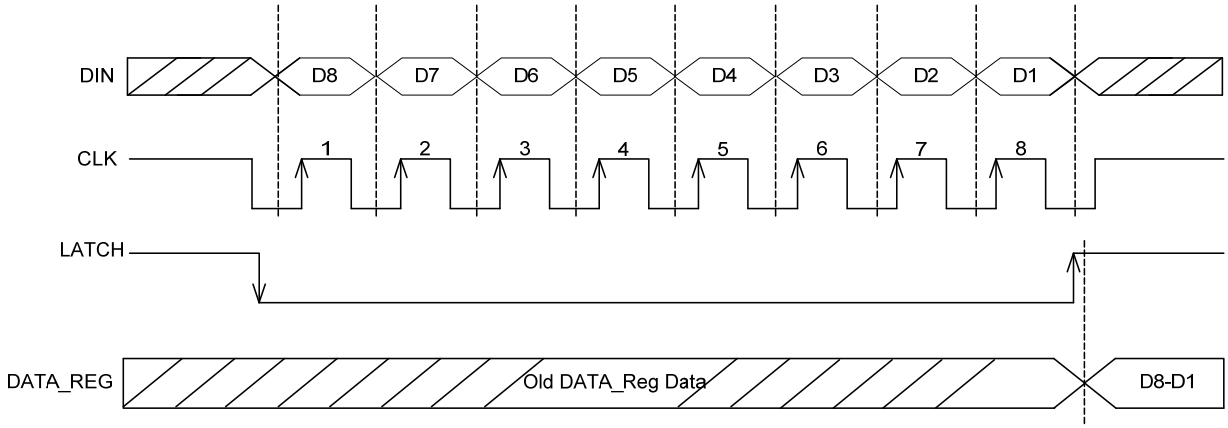


Fig 3. Writing Data Register _Single Device

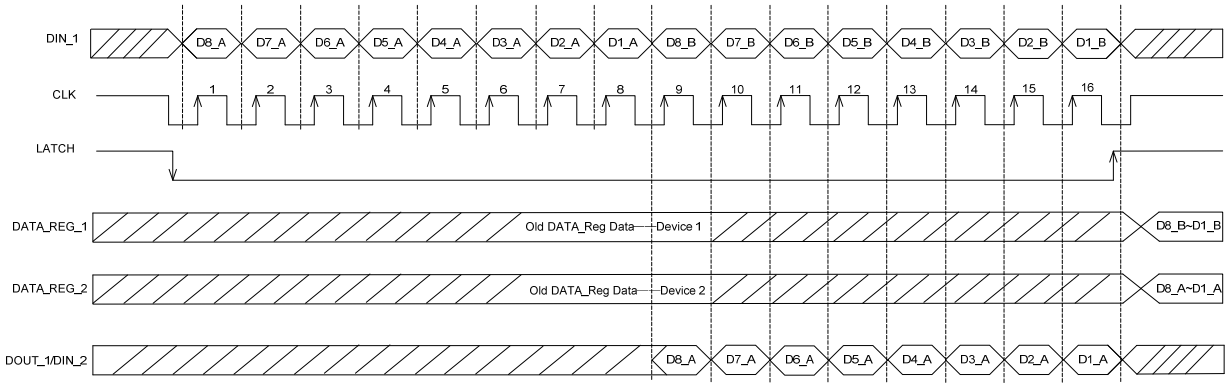


Fig 4. Writing Data Register _Daisy-Chain

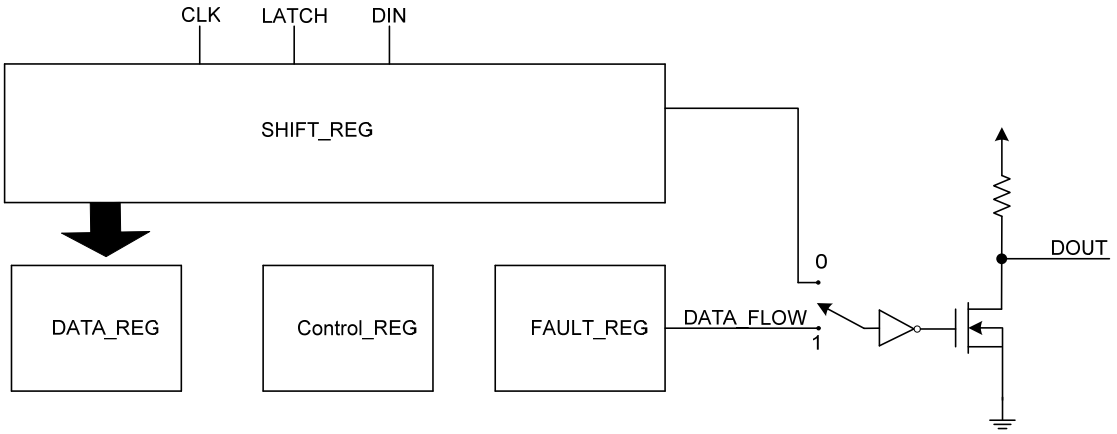


Fig 5. Writing Data Register_Data Flow

■ PROGRAMMING (Cont.)

Fault Register Reading Waveform

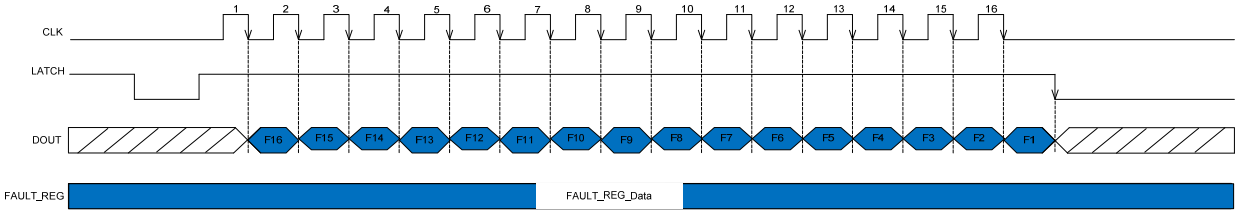


Fig 6. Reading Fault Register _Single Device

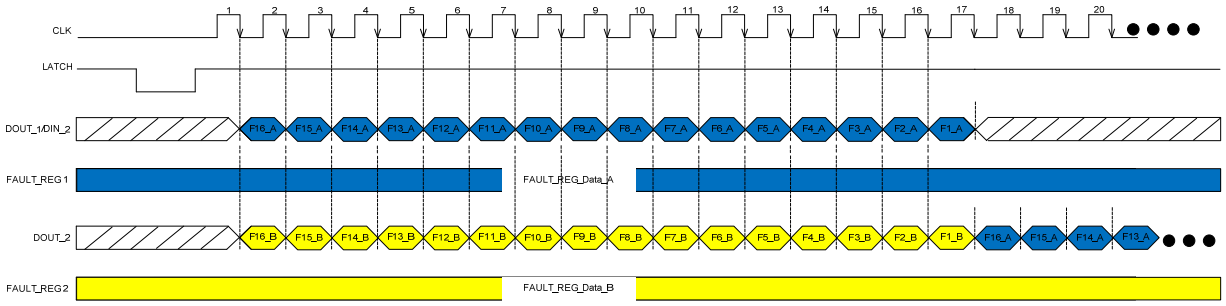


Fig 7. Reading Fault Register _Daisy-Chain

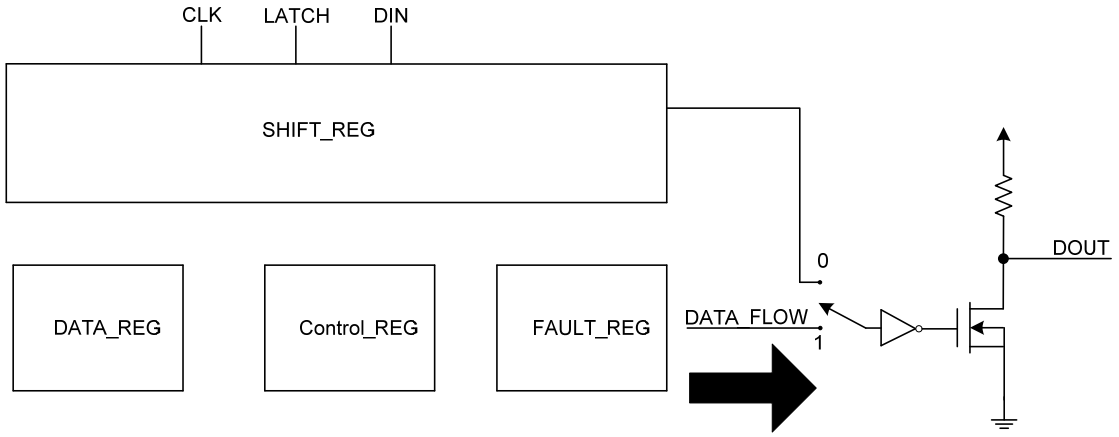


Fig 8. Reading Fault Register – Data Flow

■ PROGRAMMING (Cont.)

Special Command

Besides output ON/OFF control and fault status reading back, **U8C3060** has special functions to make system more robust or power efficient. These functions will need special command to initiate the device or configure the internal registers.

There are 5 Special Commands:

1. Write Control Register command
2. Read Control Register command
3. Read Data Register command
4. Fault Register Reset command
5. PWM Start command

Special waveform pattern on CLK and LATCH pin will issue the special command, as below

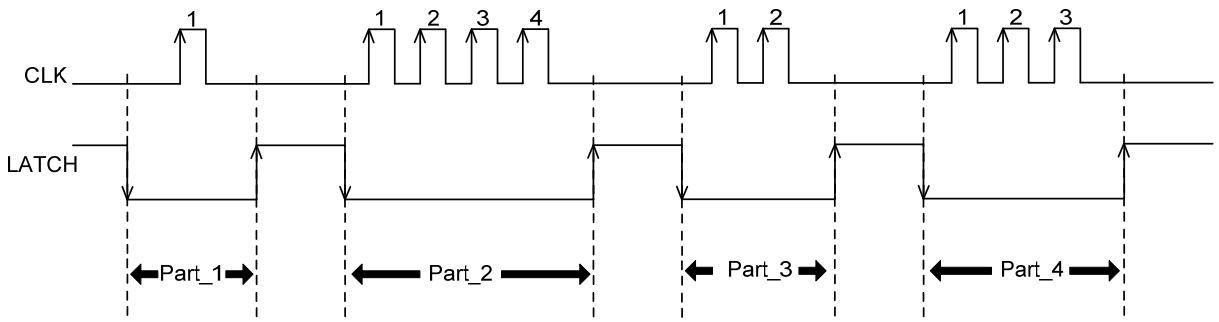


Fig 9. Special Command

Special command	CLK cycles in each part			
	Part1	Part2	Part3	Part4
Write Control Register	1	2	2	3
Read Control Register	1	4	2	3
Read Data Register	1	4	4	3
Fault Register Reset	1	2	4	3
PWM Start	1	6	6	3

■ PROGRAMMING (Cont.)

Special command: Write Control Register

When Write-Control-Register command is issued, the following serial data will be latched into timing and duty control register**.**

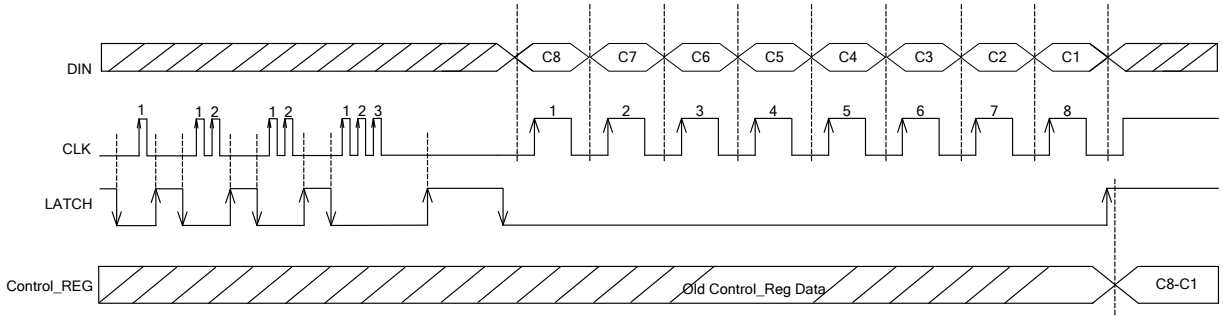


Fig 10. Writing Control Register _Single Device

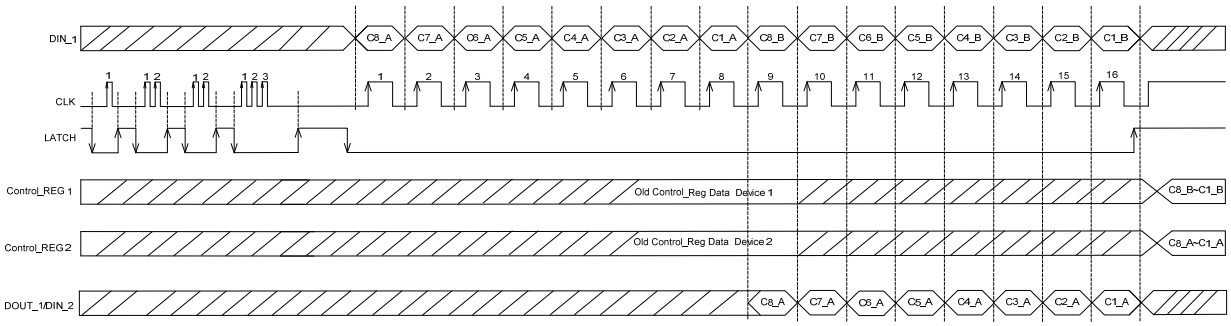


Fig 11. Writing Control Register _Daisy-Chain

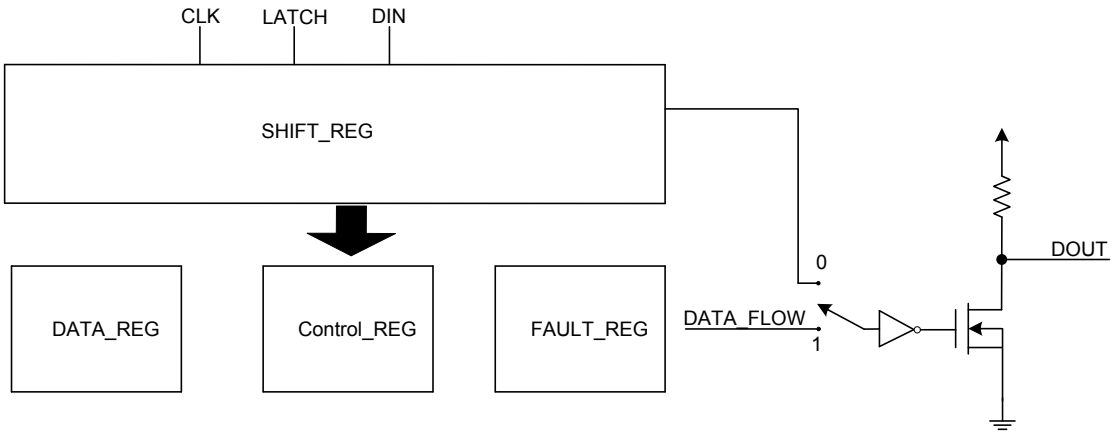


Fig 12. Writing Control Register – Data Flow

■ PROGRAMMING (Cont.)

Special command: Read Control Register

When Read-Control-Register command is issued, control register content will be copied to internal shift register and following CLK will shift this content out from DOUT pin. This provides a mechanism for system to verify the control register is correctly programmed.

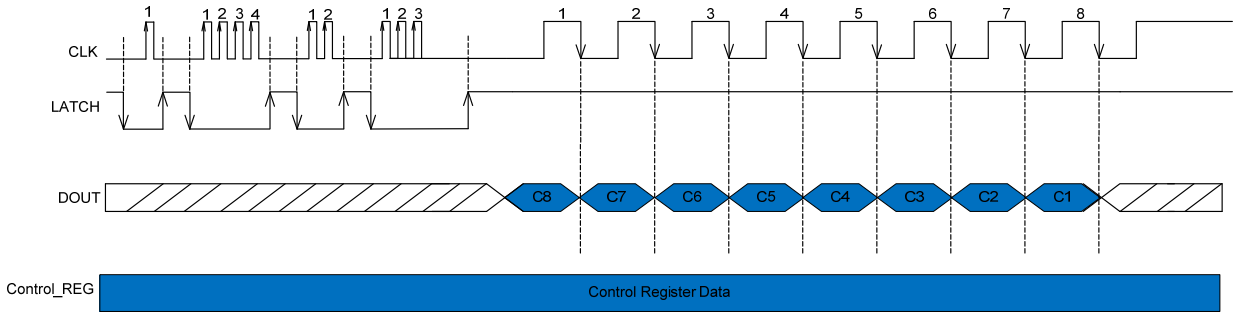


Fig 13. Reading Control Register _Single Device

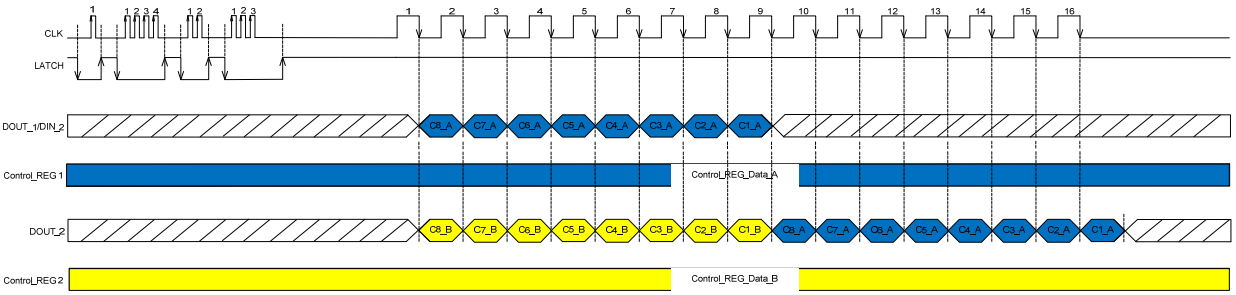


Fig 14. Reading Control Register _Daisy-Chain

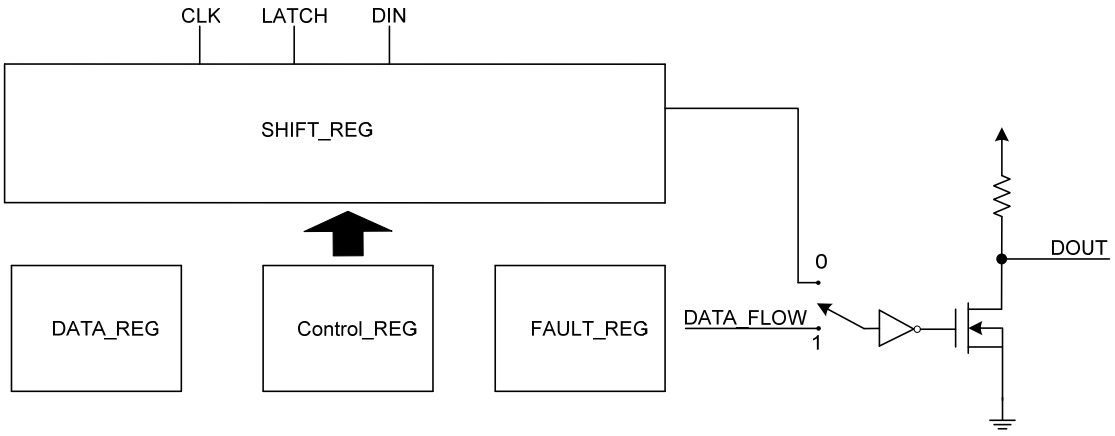


Fig 15. Read Control Register – Data Flow

■ PROGRAMMING (Cont.)

Special command: Read Data Register

When Read-Data-Register command is issued, internal output data register content will be copied to internal shift register and following CLK will shift this content out from DOUT pin. This provides a mechanism for system to verify the output data is correctly programmed. It makes system more robust in noisy system.

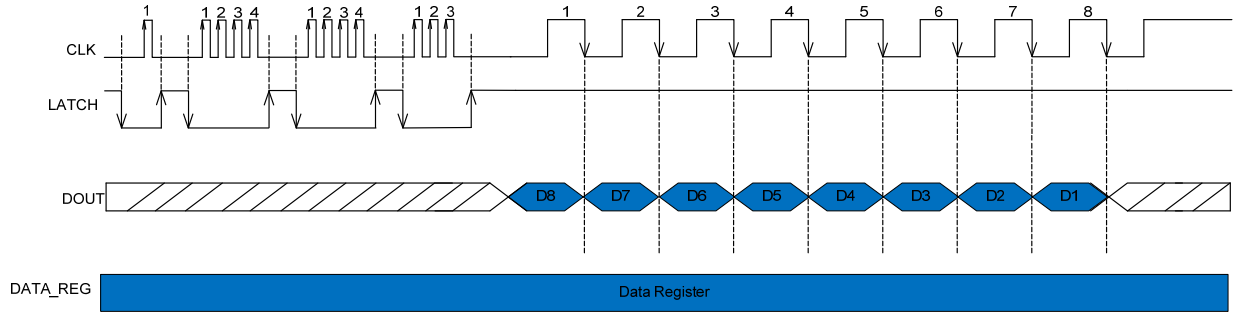


Fig 16. Reading Data Register_Single Device

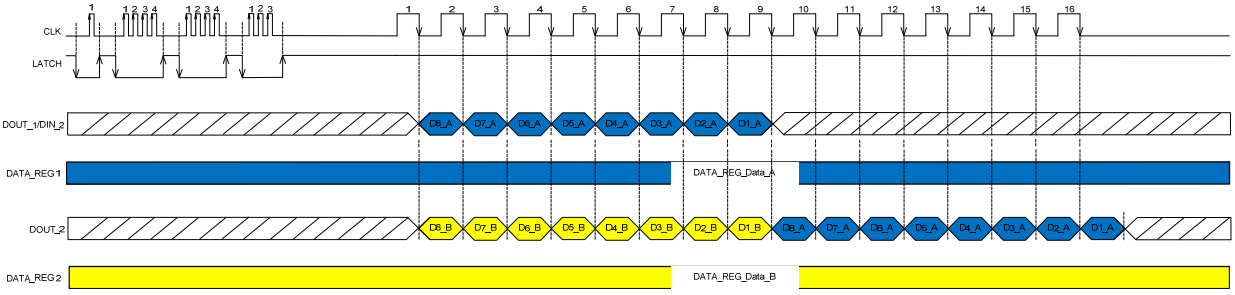


Fig 17. Reading Control Register_Daisy-Chain

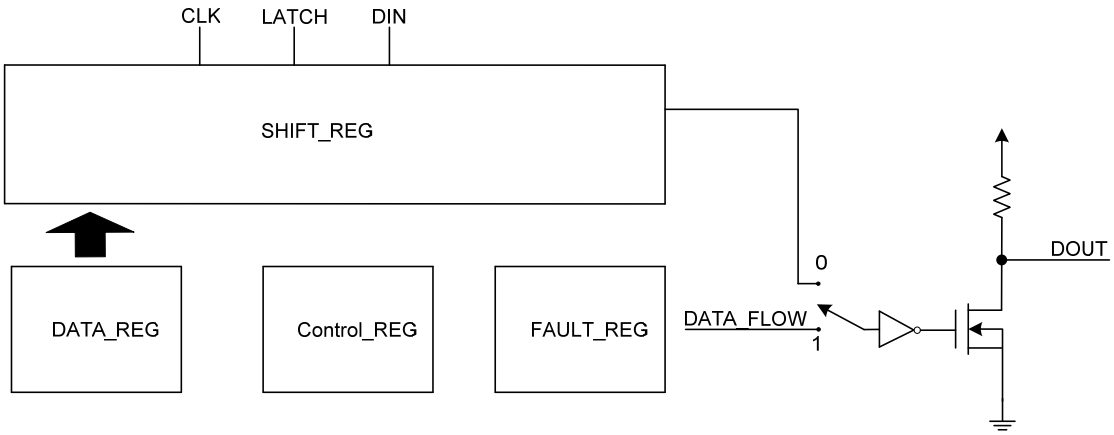


Fig 18. Reading Data Register_Data Flow

■ PROGRAMMING (Cont.)

Special command: Fault Register Reset

When Fault-Register-Reset command is issued, internal 16bit fault register will be cleared. System can use this method to clear out all fault condition in every chained device at once.

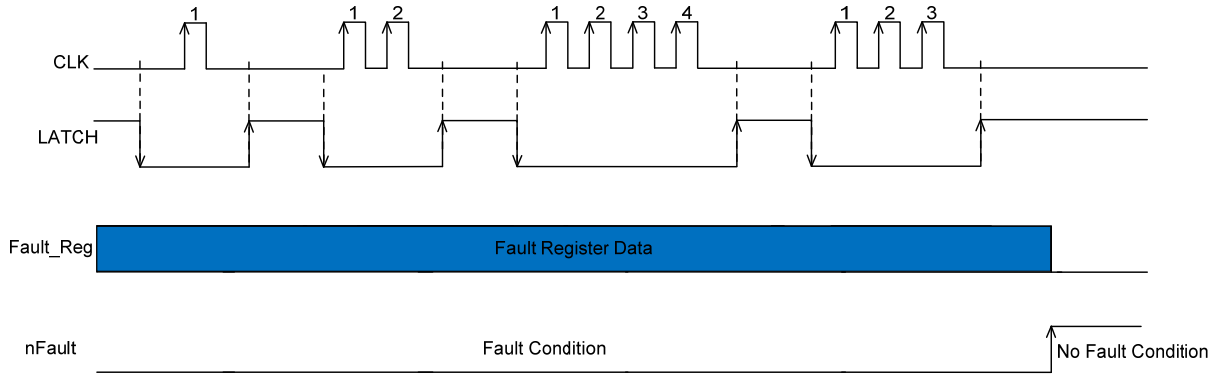


Fig 19. Fault Register Reset

Special command: PWM Start

When Fault-Register-Reset command is issued, output channel will ignore energizing time and directly enter into PWM mode following the setting in control register.

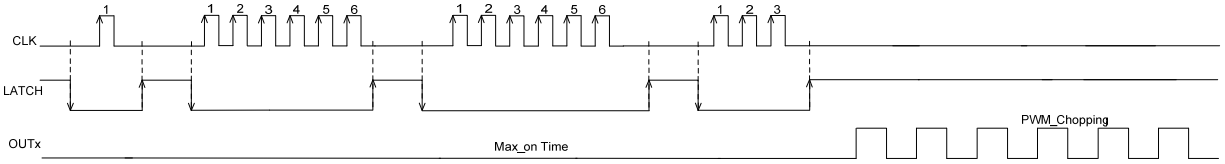


Fig 20. PWM Start Command

■ OUTPUT ENERGIZING AND PWM CONTROL

The device output is defined by two stages: Energizing Phase and PWM Phase.

During the Energizing phase, the channel is turned on with 100% duty cycle for a duration set by Control register bits C4:C1.

In PWM chopping phase, with the PWM Duty Cycle defined by Control register bits C7:C5.

The behavior of each bit in the Control Register is described in Table 8.

Table 8. Control Register Settings

DESCRIPTION		Value	C1	C2	C3	C4	C5	C6	C7	C8
Outputs always in Energizing mode		N/A	X	X	X	X	X	X	X	0
No Energizing, starts in PWM chopping		0 ms	0	0	0	0	X	X	X	1
Sets the EnergizingTime(100% duty cycle) before switching to PWM Phase		3 ms	1	0	0	0	X	X	X	1
		5 ms	0	1	0	0	X	X	X	1
		10 ms	1	1	0	0	X	X	X	1
		15 ms	0	0	1	0	X	X	X	1
		20 ms	1	0	1	0	X	X	X	1
		30 ms	0	1	1	0	X	X	X	1
		50 ms	1	1	1	0	X	X	X	1
		80 ms	0	0	0	1	X	X	X	1
		110 ms	1	0	0	1	X	X	X	1
		140 ms	0	1	0	1	X	X	X	1
		170 ms	1	1	0	1	X	X	X	1
		200 ms	0	0	1	1	X	X	X	1
		230 ms	1	0	1	1	X	X	X	1
		260 ms	0	1	1	1	X	X	X	1
		300 ms	1	1	1	1	X	X	X	1
Output is off after Energizing Phase		0 %	X	X	X	X	0	0	0	1
Sets PWM chopping duty cycle.DC is the Duty cycle that the low-side FETis on.	10kHz	12.5 %	X	X	X	X	1	0	0	1
	20kHz	25 %	X	X	X	X	0	1	0	1
	40kHz	37.5 %	X	X	X	X	1	1	0	1
		50 %	X	X	X	X	0	0	1	1
		62.5 %	X	X	X	X	1	0	1	1
		75 %	X	X	X	X	0	1	1	1
		87.5 %	X	X	X	X	1	1	1	1

■ OUTPUT ENERGIZING AND PWM CONTROL (Cont.)

There are five operation cases as described on the following sections.
The output is turned on with100% duty cycle.

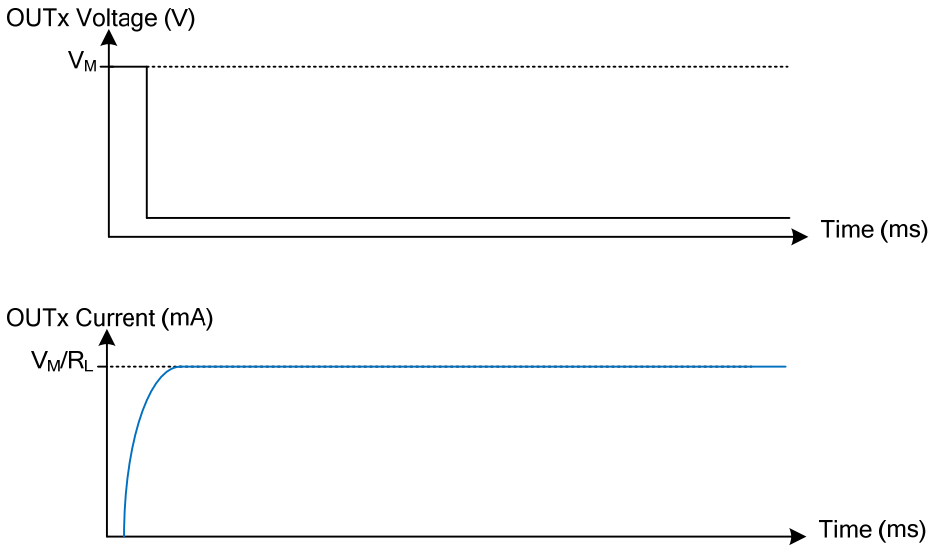


Fig 21. Case1: Timer enable bit(C8) is 0(Default value)

The output is turned on in PWM chopping mode with duty cycle defined by Control register bits C7:C5.

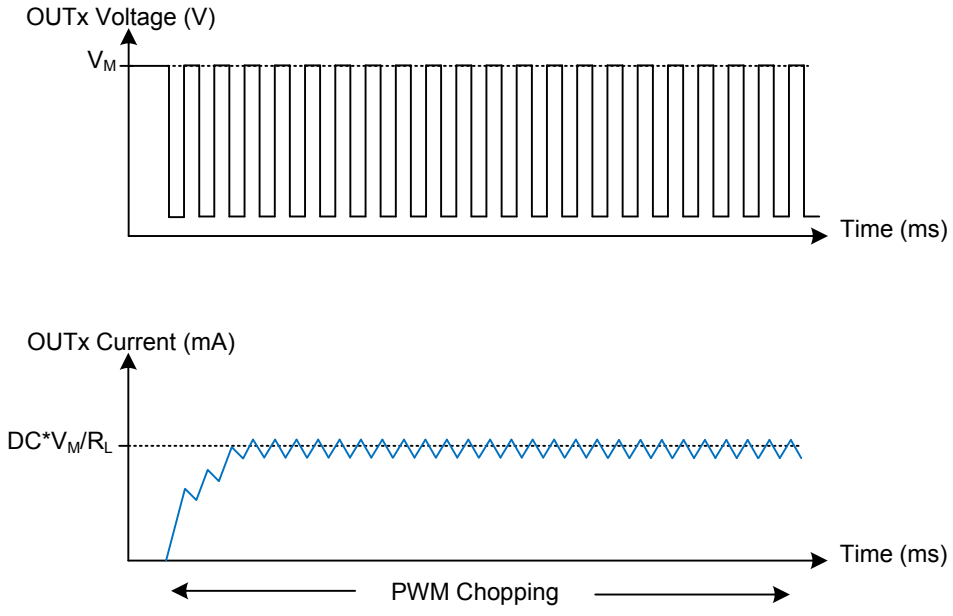


Fig 22. Case2: Timer enable bit (C8) is 1 and Energizing Timing bits (C4:C1) are 0000

■ OUTPUT ENERGIZING AND PWM CONTROL (Cont.)

The output is turned on in Energizing mode with 100% duty cycle for a duration set by Control register bits C4:C1. After the timer expires,the output switches to PWM chopping mode with PWM Duty Cycle defined by Control register bits C7:C5.

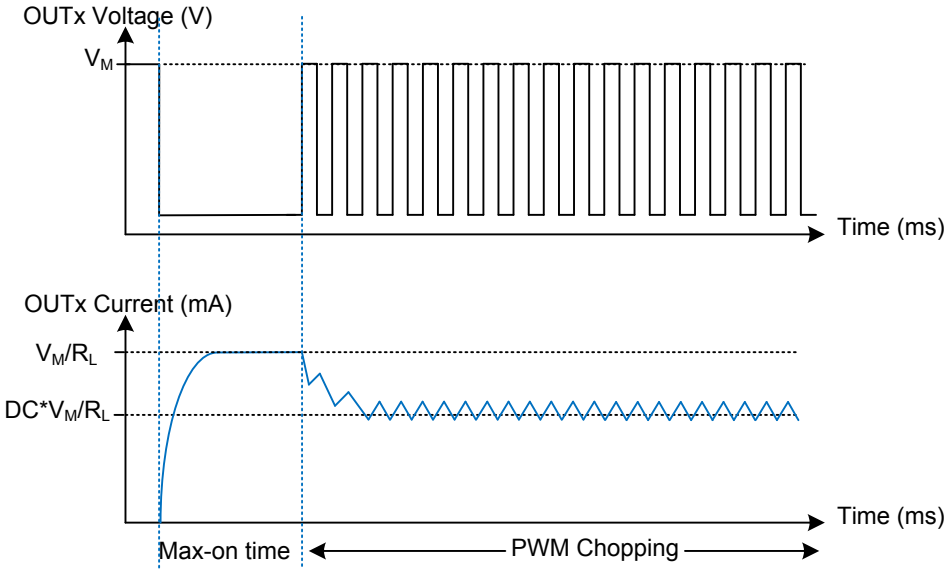


Fig 23. Case3: Timer enable bit (C8) is 1, Energizing Timing bits (C4:C1) are NOT0000, and PWM Duty bits (C7:C5) are NOT 000

The output is turned on in Energizing mode with 100% duty cycle for aduration set by Control register bits C4:C1.After the timer expires,the output is turned off.

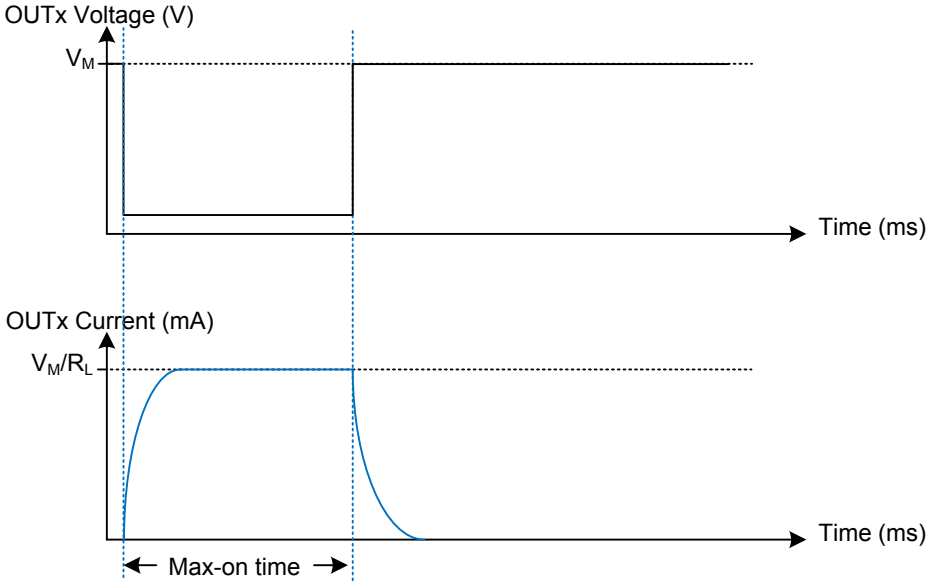


Fig 24. Case4: Timer enable bit (C8) is 1,Energizing Timing bits (C4:C1) are NOT 0000, and PWM Duty bits (C7:C5) are 000

■ APPLICATION AND IMPLEMENTATION

Application Information

The **U8C3060** is an eight channel low side driver with protection features. The following design is a common application of the **U8C3060.**

■ TYPICAL APPLICATION

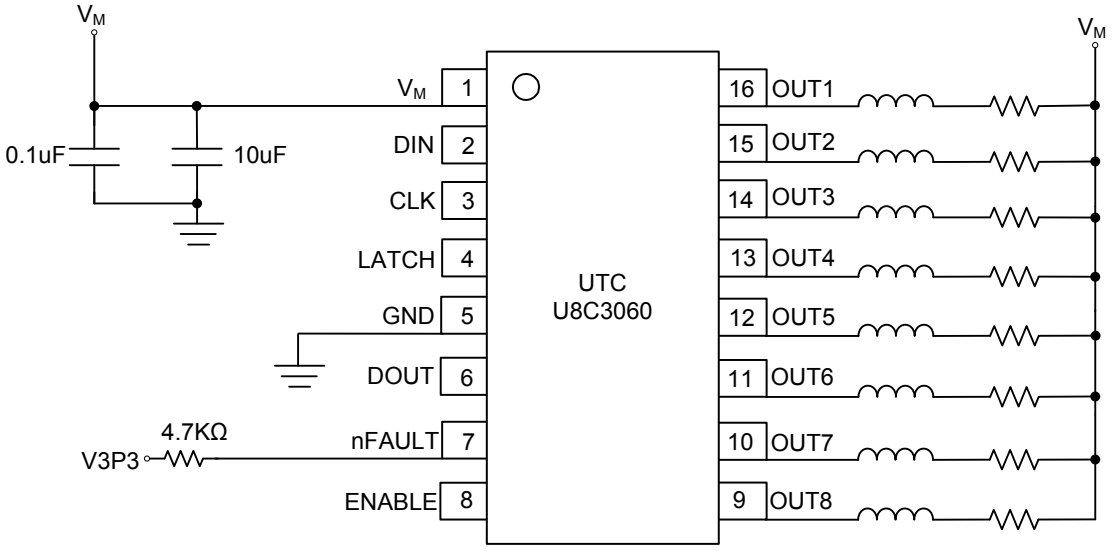


Table 9. Design Requirements

Parameter	Value
Input voltage range	8V~38V
Current	330mA per channel

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