

# UTP2012Z

# PNP EPITAXIAL SILICON TRANSISTOR

# 55V PNP LOW SATURATION MEDIUM POWER TRANSISTOR

## DESCRIPTION

The **UTP2012Z** is an PNP low  $V_{CE(SAT)}$  Breakthrough In Small Signal (BISS) transistor in a medium power.

NPN complement: UTN2010Z.

## FEATURES

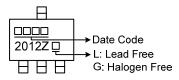
- \* Very low collector-emitter saturation voltage V<sub>CE(SAT)</sub>
- \* High collector current capability IC and ICM
- \* High collector current gain  $(h_{FE})$  at high IC
- \* High energy efficiency due to less heat generation
- \* Smaller required Printed-Circuit Board (PCB) area than for conventional transistors

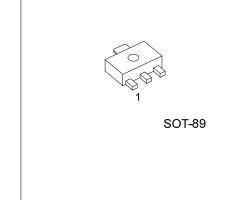
## ORDERING INFORMATION

Ordering Number		Dookago	Pin Assignment			Dooking
Lead Free	Halogen Free	Package	1	2	3	Packing
UTP2012ZL-AB3-R	UTP2012ZG-AB3-R	SOT-89	В	С	E	Tape Reel
Note: Pin Assignment: B: Bas	e C: Collector E: Emitt	er				

UTP2012Z <u>G-AB3-R</u>		
	(1)Packing Type	(1) R: Tape Reel
	(2)Package Type	(2) AB3: SOT-89
	(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

### MARKING





### ■ ABSOLUATE MAXIUM RATINGS (T<sub>A</sub>= 25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Collector to Base Voltage	V <sub>CBO</sub>	-100	V
Collector to Emitter Voltage	V <sub>CEO</sub>	-55	V
Emitter to Base Voltage	V <sub>EBO</sub>	-7	V
Bese Current	Ι <sub>Β</sub>	-2	А
Collector Current	Ι <sub>C</sub>	-4.3	А
Peak Collector Current (t <sub>P</sub> ≤1ms)	I <sub>СМ</sub>	-15	А
Collector Dissipation	Pc	1.5	W
Junction Temperature	TJ	-40 ~ +150	°C
Storage Temperature	T <sub>STG</sub>	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Single pulse, P<sub>W</sub>=10ms.

3. Device mounted on FR-4 PCB with minimum recommended pad layout. (25×25×1.6mm)

#### THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT		
Junction to Ambient	θ <sub>JA</sub>	83	°C/W		
Note : Device mounted on EP.4 PCB with minimum recommended pad layout (25x25x1 6mm)					

Note : Device mounted on FR-4 PCB with minimum recommended pad layout. (25×25×1.6mm).

#### ■ **ELECTRICAL CHARACTERISTICS** (T<sub>A</sub>= 25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Collector-Base Breakdown Voltage	$BV_{CBO}$	I <sub>C</sub> =-100μA	-100			V
Collector-Emitter Breakdown Voltage	$BV_{CER}$	I <sub>C</sub> =-1μA, RB≤1kΩ	-100			V
Collector-Emitter Breakdown Voltage	$BV_{CEO}$	I <sub>C</sub> =-10mA	-55			V
Emitter-Base Breakdown Voltage	$BV_{EBO}$	I <sub>E</sub> =-100μA	-7.0			V
	I <sub>CBO</sub>	V <sub>CB</sub> =-80V, I <sub>E</sub> =0A			-20	nA
Collector-Base Cut-off Current		V <sub>CB</sub> =-80V, I <sub>E</sub> =0A, T <sub>A</sub> =100°C			-500	nA
Collector-Emitter Cut-off Current	I <sub>CER</sub>	V <sub>CE</sub> =-80V, RB≤1kΩ			-20	nA
Emitter-Base Cut-off Current	I <sub>EBO</sub>	V <sub>EB</sub> =-6V, I <sub>C</sub> =0A			-10	nA
Base-Emitter On Voltage (Note)	V <sub>BE (ON)</sub>	V <sub>CE</sub> =-1V, I <sub>C</sub> =-5A			-950	mV
Base-Emitter Saturation Voltage (Note)	$V_{\text{BE}(\text{SAT})}$	I <sub>C</sub> =-5Α, I <sub>B</sub> =-500mA			-1050	mV
Collector-Emitter Saturation Voltage (Note)	V <sub>CE(SAT)</sub>	I <sub>C</sub> =-100mA, I <sub>B</sub> =-10mA			-20	mV
		I <sub>C</sub> =-1A, I <sub>B</sub> =-100mA			-65	mV
		I <sub>C</sub> =-2A, I <sub>B</sub> =-200mA			-110	mV
		I <sub>C</sub> =-5Α, I <sub>B</sub> =-500mΑ			-300	mV
DC Current Transfer Ratio (Note)	h <sub>FE</sub>	I <sub>C</sub> =-10mA, V <sub>CE</sub> =-1V	100			
		I <sub>C</sub> =-2A, V <sub>CE</sub> =-1V	100		300	
		I <sub>C</sub> =-5A, V <sub>CE</sub> =-1V	45			
		I <sub>C</sub> =-10A, V <sub>CE</sub> =-1V	10			
Transition Frequency (Note)	f⊤	I <sub>C</sub> =-100mA, V <sub>CE</sub> =-10V, f=50MHz		120		MHz
Collector Capacitance	C <sub>OB</sub>	V <sub>CB</sub> =-10V, f=1MHz		90		рF

Note : Measured under pulsed conditions. Pulse Test: Pulse width  $\leq$  300µs, Duty cycle  $\leq$  2%.



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