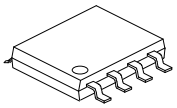
CURRENT MODE PWM CONTROLLER FOR FORWARD AND FLYBACK APPLICATIONS



SOP-8

■ DESCRIPTION

The UTC **UC3853A** is a high performance current mode PWM controller ideally suited for low standby power. Low V_{DD} startup current make the power reliable on startup design and a large value resistor could be used to minimize the standby power. At no load condition, the IC operates in power-saving mode for lower standby power, decreasing frequency for Higher conversion efficiency at light load condition. It contains protection with automatic recovery including OLP, OCP, V_{CC} OVP, BNO and OTP. To protect the power MOSFET, Gate-drive output is fixed up to 15V max.

Excellent EMI performance is achieved with UTC proprietary frequency hopping technique (ZL201020615247.1) together with soft driver control. The controller offers everything needed to build cost−effective and reliable ac−dc switching supplies dedicated to ATX power supplies. Finally a SOP-8 package saves PCB space and represents a solution of choice in cost sensitive project.

■ FEATURES

* Peak Current Mode Control
* Adjustable Switching Frequency
* Adjustable Soft−start Timer
* Adjustable Internal Ramp Compensation
* Jittering Frequency ±6% of the Switching Frequency
* Power-saving mode for high standby efficiency
* Auto−recovery Primary OCP with 10ms Fixed Delay
* Auto−recovery Brown−Out Detection
* Delayed Operation Upon Start−up via an Internal Fixed Timer
* UC384X−like UVLO Thresholds
* V_{CC} from 9V to 28V with Auto−recovery UVLO
* Internal 350ns Leading Edge Blanking
* Gate output voltage clamped at 15V
* UC3853A: Maximum 47% Duty Cycle

■ ORDERING INFORMATION

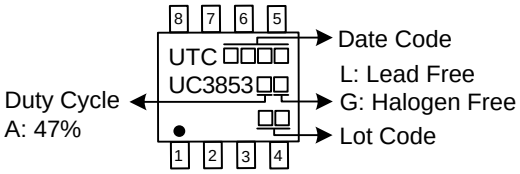
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UC3853AL-S08-R	UC3853AG-S08-R	SOP-8	Tape Reel

UC3853AG-S08-R

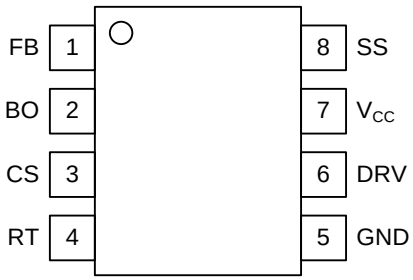
(1)Packing Type
(2)Package Type
(3)Green Package
(4)Duty Cycle

(1) R: Tape Reel
(2) S08: SOP-8
(3) G: Halogen Free and Lead Free, L: Lead Free
(4) A: 47%

■ MARKING



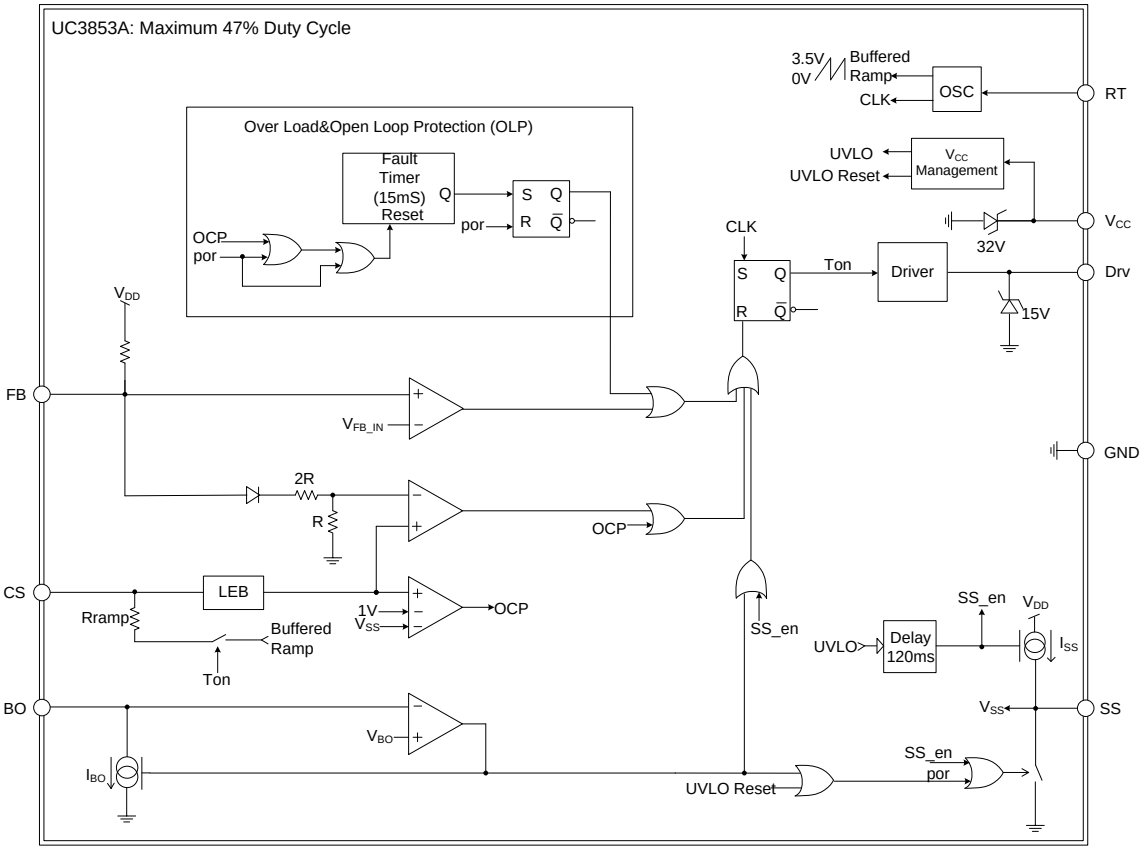
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	FB	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and SENSE pin input
2	BO	Line input voltage brown out protection
3	CS	Current sense input pin. Connected to MOSFET current sensing resistor node
4	RT	A resistor connected to ground defined the switching frequency
5	GND	Ground
6	DRV	This pin connects to the MOSFET gate
7	V_{CC}	Power supply
8	SS	A capacitor connected to ground defined the soft start time

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply Voltage, V_{CC} Pin, OVP Voltage	V_{CC}	29	V
Power Supply Voltage, V_{CC} Pin, Continuous Voltage	V_{CC}	28	V
Maximum Current Injected Into Pin 7	I_{VCC}	20	mA
Maximum Voltage On Low Power Pins (Except pin 6, 7)		-0.3 ~ 10	V
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{OPR}	-60 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Typical Thermal Resistance	θ_{JA}	169	°C/W

■ ELECTRICAL DATA

(V_{CC}=15V, R_T=43kΩ, C_{DRV}=1nF. For typical values T_J=25°C, for min/max values T_J=–25°C~+125°C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY SECTION AND V_{CC} MANAGEMENT						
Startup Threshold At Which Driving Pulses Are Authorized	V_{CC_ON}	V_{CC} increasing	9.4	10	10.6	V
Minimum Operating Voltage At Which Driving Pulses Are Stopped	V_{CC_OFF}	V_{CC} decreasing	8.3	9	9.6	V
Start−up Current, Controller Disabled	I_{STR}	V_{CC}<$V_{CC(on)}$&V_{CC} increasing from zero		5	20	μA
Internal IC Consumption, Controller Switching	I_{CC}	FB=3.5V, R_T=43kΩ	0.5	1.1	2	mA
OVP Threshold	V_{CC_OVP}	FB=3.5V，R_T=43KΩ	26.5	28.5	30.5	V
CURRENT COMPARATOR						
Current Sense Voltage Threshold	V_{ILIM}		0.89	0.96	1.04	V
Leading Edge Blanking Duration	t_{LEB}	(Note 1)		350		ns
Internal Ramp Compensation Voltage Level	V_{Ramp}	@ 25°C (Note 2)	3.15	3.5	3.85	V
Internal Ramp Compensation Resistance To CS Pin	R_{Ramp}	@ 25°C (Note 2)		26.5		kΩ
INTERNAL OSCILLATOR						
Oscillator Frequency	f_{OSC}	R_T=43kΩ & DRV pin=47kΩ	90	100	110	kHz
Frequency Modulation In Percentage Of f_{OSC}	f_{Jitter}	(Note 1)		±6		%
Maximum Duty Cycle	$DC_{\_Max.}$	UC3853A	42	46	50	%
FEEDBACK SECTION						
Internal Voltage Division From FB To CS Setpoint	FB_{DIV}	(Note 1)		3		
Internal Pull−Up Resistor	$R_{Pull-up}$	(Note 1)		3.5		kΩ
FB Pin Maximum Current	I_{FB}	FB pin=GND	1			mA
Open Loop Feedback Voltage	V_{FBOL}	FB pin=OPEN		5.4		V
Burst-Mode Enter FB Voltage	V_{FB-IN}			0.63		V
Burst-Mode Quit FB Voltage	V_{FB-OUT}			0.66		V

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVE OUTPUT						
Output Voltage Low State	V_{OL}	I_{SOURCE}=20mA			0.8	V
Output Voltage High State	V_{OH}	I_{SINK}=20mA	10			V
Output Voltage Rise Time	t_R	C_L=1.0nF	60	120	260	ns
Output Voltage Fall Time	t_F	C_L=1.0nF	30	60	100	ns
Output Clamp Voltage	V_{Clamp}			15		V
SOFT START						
Soft−Start Charge Current	I_{SS}	SS pin=GND	8	10	12	μA
Soft Start Completion Voltage Threshold	V_{SS}		3.5	4.0	4.5	V
Internal Delay Before Starting The Soft Start When $V_{CC(on)}$ Is Reached	SS_{Delay}		70	120	180	ms
PROTECTION						
Current Sense Fault Voltage Level Triggering The Timer	F_{CS}		0.89	0.96	1.04	V
Timer Delay Before Latching A Fault (Overload Or Short Circuit)	T_{Fault}	When CS pin>F_{CS}	10	20	40	ms
Brown−Out Voltage	V_{BO}		0.89	0.96	1.04	V
PROTECTION						
Internal Current Source Generating The Brown−Out Hysteresis	I_{BO}		9.2	10	10.8	μA

Notes: 1. Guaranteed by design.
2. V_{ramp}, R_{ramp} Guaranteed by design.

■ APPLICATION INFORMATION

Introduction

The UTC **UC3853A** hosts a high−performance current−mode controller specifically developed to drive power supplies designed for the ATX and the adapter market:

Current Mode operation

Implementing peak current−mode control topology, the circuit offers UC384X−like features to build rugged power supplies.

Adjustable switching frequency

A resistor to ground precisely sets the switching frequency.

Internal frequency jittering

Frequency jittering softens the EMI signature by spreading out peak energy within a band ±6% from the center frequency.

Wide V_{CC} excursion

The controller allows operation up to 28V continuously and IC will be shutdown when $\mathbf{V_{CC}}$ transient voltage up to 29V.

Gate drive clamping

The controller includes a low−loss clamping voltage which prevents the gate from going beyond 15V typical.

Low startup−current

The start−up current is guaranteed to be less than 5μA maximum, helping the designer to reach a low standby power level.

Open Loop&Over Load&Short−circuit protection

When V_{CS} exceeds 0.96V , the controller detects a fault and starts an internal digital timer. On the condition that the digital timer elapses 20mS, the controller will shutdown. Reset occurs when: a) a BO reset is sensed, b) V_{CC} is cycled down to $V_{CC(min)}$ level.

Adjustable soft−start

The soft−start is activated upon a start−up sequence after a minimum internal time delay of 120m (SS_{delay}). But also when the brown−out pin is reset without in that case timer delay. The soft start pin I grounded until the internal delay is ended.

Shutdown

if an external transistor brings the BO pin down, the controller is shut down, but all internal biasing circuits are alive. When the pin is released, a new soft−start sequence takes place.

Brown−Out protection

When BO pin voltage is below the V_{BO} threshold, the circuit stays off and does not switch. When BO pin voltage comes back within safe limits, the pulses are re−started via a start−up sequence including soft−start. The hysteresis I implemented via a current source connected to the BO pin, which sinks a current (I_{BO}) from the pin to the ground. it can easily be used for hysteresis purposes.

Internal ramp compensation

A resistor connected from the CS pin to the sense resistor allows the designer to inject ramp compensation inside his design.

■ APPLICATION INFORMATION (Cont.)

Burst mode

If the output loads disappear, the FB is allowed to decreases down to V_{FB_IN}, zero duty cycle is imposed. This mode helps to ensure no−load outputs conditions as requested by recently updated ATX specifications. Bust mode easily obtains 100mW standby power. The following figure illustrates the different mode of operation versus the FB pin level.

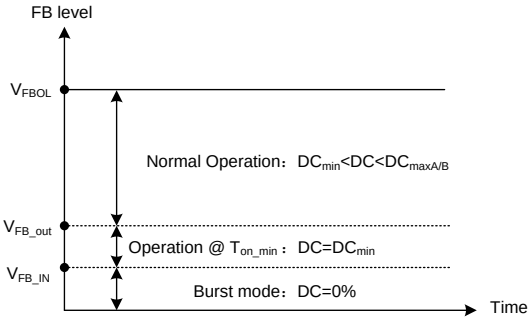


Figure 1. Mode Of Operation Versus The FB Pin Level

Startup Sequence

The startup sequence is activated when Vcc pin reaches $V_{CC(on)}$ level，and the internal delay timer (SS_{delay}) runs. Only when the internal delay end，the soft start can be allowed if the BO pin level is above V_{BO} level. The soft start is allowed if the BO pin threshold is reached，and the voltage on the SS pin is rising from the ground. An external capacitor connected on SS pin is used to defined SS time. The voltage variation of the SS pin divided by 4 gives the peak current variation on the CS pin.

The following figures illustrate the different startup cases.

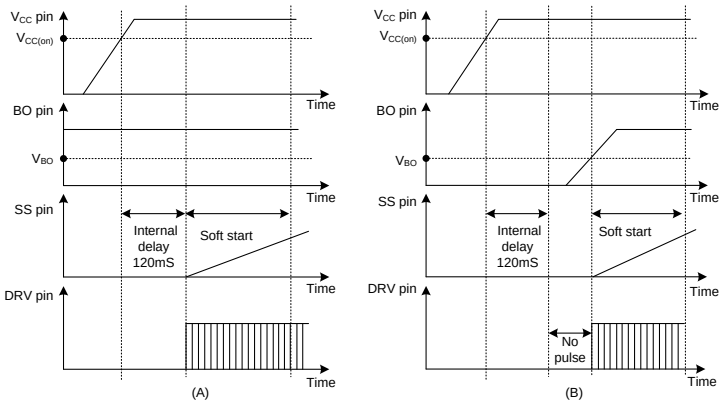


Figure 2. Startup Sequence (A) & (B)

■ APPLICATION INFORMATION (Cont.)

For the (A), when the V_{CC} pin reaches the $V_{CC(on)}$ level, the internal timer starts. As the BO pin level is above the V_{BO} threshold at the end of the internal delay, a soft start sequence is started. For the (B), at the end of the internal delay, the BO pin level is below the V_{BO} threshold thus the soft start sequence can not start. A new soft start sequence will start only when the BO pin reaches the V_{BO} threshold.

When the BO pin is grounded, the controller is shut down and the SS pin is internally grounded. If the BO pin is released, a new soft start sequence happens after its level reaches the V_{BO} level.

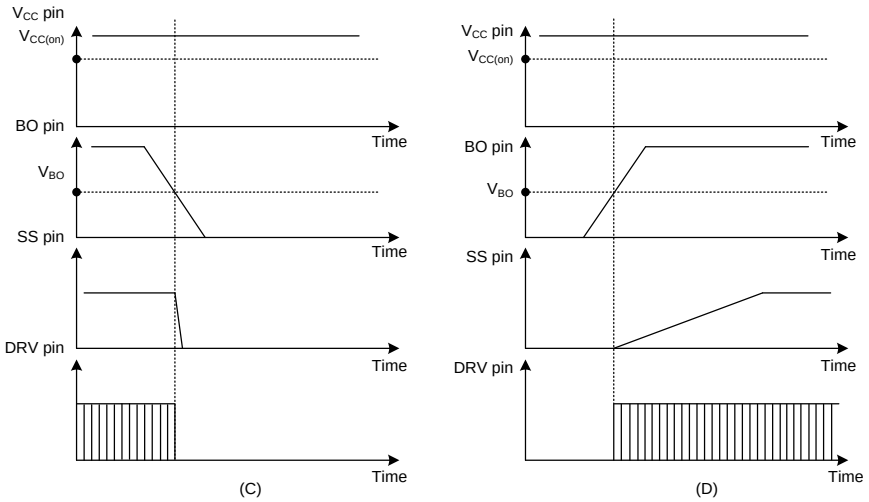


Figure 3. Brown Out Protection

Soft Start

As illustrated by the following figure, the rising voltage on the SS pin voltage divided by 4 controls the peak current sensed on the CS pin. Thus as soon as the CS pin voltage becomes higher than the SS pin voltage divided by 4 the driver is off cycle by cycle.

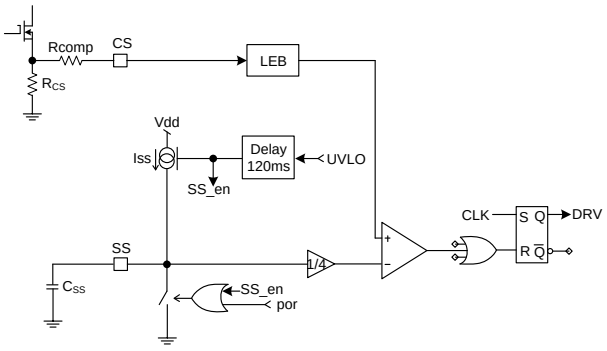


Figure 5. Soft Start

■ APPLICATION INFORMATION (Cont.)

The following figure illustrates a soft start sequence.

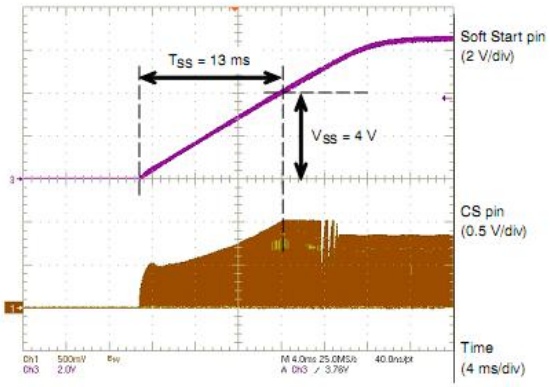


Figure 6. Soft Start Example

Brown−Out Protection

The controller protects converter against low input voltage conditions by monitoring the Voltage on BO pin. When the BO pin voltage falls below the V_{BO}, the controllers stops pulsing until the input level goes back to normal and resumes the operation via a new soft start sequence.The hysteresis is implemented by using the internal current connected between the BO pin and the ground when the BO pin is below the V_{BO}.

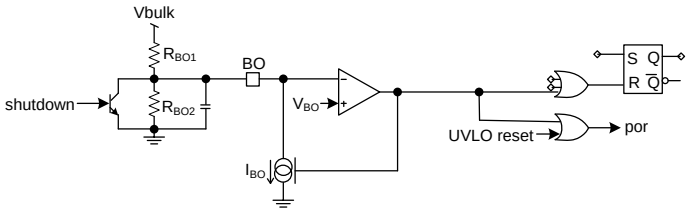


Figure 7. BO Pin Setup

The following equations show how to calculate the resistors for BO pin. First of all, select the bulk voltage value at which the controller must start switching (V_{bulkon}) and the bulk voltage for shutdown ($V_{bulkoff}$) the controller. Where: V_{bulkon}=370V, $V_{bulkoff}$=350V, V_{BO}=0.96V, I_{BO}=9.8μA. When BO pin voltage is below V_{BO}, the internal current source (I_{BO}) is activated. The following equation can be written:

$$V_{bulk\,ON} = R_{BO1}\left(I_{BO} + \frac{V_{BO}}{R_{BO2}}\right) + V_{BO} \qquad \text{(eq. 1)}$$

■ APPLICATION INFORMATION (Cont.)

When BO pin voltage is higher than V_{BO}, the internal current source is now disabled. The following equation can be written:

$$V_{BO} = \frac{V_{bulkoff} R_{BO2}}{R_{BO2} + R_{BO1}} \quad \text{(eq. 2)}$$

From Equation 2 it can be extracted the R_{BO1}:

$$R_{BO1} = \left(\frac{V_{bulkoff} - V_{BO}}{V_{BO}} \right) R_{BO2} \quad \text{(eq. 3)}$$

Equation 3 is substituted in Equation 1 and solved for R_{BO2}, yields:

$$R_{BO2} = \frac{V_{BO}}{I_{BO}} \left(\frac{V_{bulkon} - V_{BO}}{V_{bulkoff} - V_{BO}} - 1 \right) \quad \text{(eq. 4)}$$

R_{BO1} can be also written independently of R_{BO2} by substituting Equation 4 into Equation 3 as follow:

$$R_{BO1} = \frac{V_{bulkon} - V_{bulkoff}}{I_{BO}} \quad \text{(eq. 5)}$$

From Equation 4 and Equation 5, the resistor divider value can be calculated:

$R_{BO2} = \frac{0.96}{9.8\mu} \left(\frac{370 - 0.96}{350 - 0.96} - 1 \right) = 5613\Omega$, $R_{BO1} = \frac{370 - 350}{9.8\mu} = 2.04M\Omega$

Short Circuit or Open Loop&Over Load Protection

A short circuit or an open loop&overload situation is detected when the CS pin voltage reaching 0.96V. If the condition continued for 15ms, the fault is latched and the controller permanently stops the pulses on the driver pin.

If the fault is latched the controller can be reset if a BO reset is sensed or if V_{CC} is cycled down to $V_{CC(off)}$.

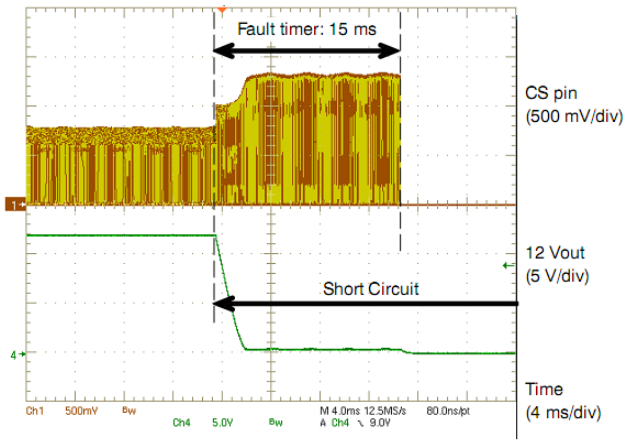


Figure 8. Short Circuit Detection Example

Shut Down

There is one possibility to shut down the controller; this possibility consists at grounding the BO pin as illustrated in Figure 7.

■ APPLICATION INFORMATION (Cont.)

Ramp Compensation

Ramp compensation is a known mean to cure subharmonic oscillations. These oscillations take place at half of the switching frequency and occur only during CCM with a duty−cycle above 50%. To lower the current loop gain, one usually injects between 50 and 100% of the inductor down slope.The ramp compensation applied on CS pin is from the internal oscillator ramp buffered. A switch placed between the buffered internal oscillator ramp and R_{ramp} disconnects the ramp compensation during the off time Ton signal.

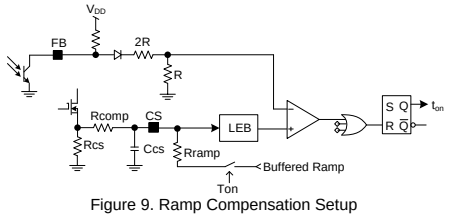


Figure 9. Ramp Compensation Setup

In the UTC **UC3853A**, the internal ramp swings with a slope of:

$$S_{int} = \frac{V_{ramp}}{DC_{max}} F_{SW} \qquad \text{(eq. 6)}$$

In a forward application the secondary−side downslope viewed on a primary side requires a projection over the sense resistor R_{sense}. Thus:

$$S_{CS} = \frac{(V_{out} + V_f)}{L_{out}} \frac{N_s}{N_p} R_{CS} \qquad \text{(eq. 7)}$$

where:

- V_{out} is output voltage level
- V_f the freewheel diode forward drop
- L_{out}, the secondary inductor value
- N_s/N_p the transformer turn ratio
- R_{CS}: the sense resistor on the primary side

Assuming the selected amount of ramp compensation to be applied is δ_{comp}, then we must calculate the division ratio to scale down S_{int} accordingly:

$$Ratio = \frac{R_{CS}\delta_{comp}}{S_{int}} \qquad \text{(eq. 8)}$$

A few line of algebra determined R_{comp} :

$$R_{comp} = R_{ramp} \frac{Ratio}{1 - Ratio} \qquad \text{(eq. 9)}$$

The previous ramp compensation calculation does not take into account the natural primary ramp created by the transformer magnetizing inductance. In some case illustrated here after the power supply does not need additional ramp compensation due to the high level of the natural primary ramp.

The natural primary ramp is extracted from the following formula:

$$S_{natural} = \frac{V_{bulk}}{L_{mag}} R_{CS} \qquad \text{(eq. 10)}$$

Then the natural ramp compensation will be:

$$\delta_{natural\_comp} = \frac{S_{natural}}{S_{CS}} \qquad \text{(eq. 11)}$$

If the natural ramp compensation ($\delta_{natural\_comp}$) is higher than the ramp compensation needed (δ_{comp}), the power supply does not need additional ramp compensation. If not, only the difference ($\delta_{comp} - \delta_{natural\_comp}$) should be used to calculate the accurate compensation value.

Thus the new division ratio is:

$$\text{If } \delta_{natural\_comp} < \delta_{comp} \Rightarrow Ratio = \frac{S_{CS}(\delta_{comp} - \delta_{natural\_comp})}{S_{int}} \qquad \text{(eq. 12)}$$

Then R_{comp} can be calculated with the same equation used when the natural ramp is neglected (Equation 9).

■ APPLICATION INFORMATION (Cont.)

Ramp Compensation Design Example

2 switch−Forward Power supply specification:

- Regulated output: 12V
- L_{out}=27μH
- V_f=0.62V (drop voltage on the regulated output)
- Current sense resistor: 0.75Ω
- Switching frequency: 100kHz
- V_{bulk}=350V, minimum input voltage at which the power supply works.
- Duty cycle max: DC_{max}=75%
- V_{ramp}=3.5V, Internal ramp level.
- R_{ramp}=26.5kΩ, Internal pull−up resistance
- Targeted ramp compensation level: 100%
- Transformer specification: L_{mag}=13mH, N_s/N_p=0.085 Internal ramp compensation level

$$S_{int}=\frac{V_{ramp}}{DC_{max}}F_{SW}\Rightarrow S_{int}=\frac{3.5}{0.75}*100kHz=467mV/\mu S$$

Secondary−side downslope projected over the sense resistor is:

$$S_{CS}=\frac{(V_{out}+V_f)}{L_{out}}\frac{N_s}{N_p}R_{CS}\Rightarrow S_{CS}=\frac{(12+0.7)}{27*10^{-6}}0.085*0.75=30mV/\mu S$$

Natural primary ramp:

$$S_{natural}=\frac{V_{bulk}}{L_{mag}}R_{CS}\Rightarrow S_{natural}=\frac{350}{13\bullet 10^{-3}}*0.75=20.19mV/\mu S$$

Thus the natural ramp compensation is:

$$\delta_{natural\_comp}=\frac{S_{natural}}{S_{CS}}\Rightarrow \delta_{natural\_comp}=\frac{20.19}{30}=67.3\%$$

■ APPLICATION INFORMATION (Cont.)

Here the natural ramp compensation is lower than the desired ramp compensation, so an external compensation should be added to prevent sub−harmonics oscillation.

$$\text{Ratio}=\frac{S_{CS}(\delta_{comp}-\delta_{natural\_comp})}{S_{int}} \Rightarrow \text{Ratio}=\frac{30*(1.00-0.673)}{467}=0.021$$

We can know calculate external resistor (R_{comp}) to reach the correct compensation level.

$$R_{comp}=R_{ramp}\frac{\text{Ratio}}{1-\text{Ratio}} \Rightarrow R_{comp}=26.5*10^{3}*\frac{0.021}{1-0.021}=568.4\Omega$$

Thus with Rcomp = 570Ω, 100% compensation ramp is applied on the CS pin.

The following example illustrates a power supply where the natural ramp offers enough ramp compensation to avoid external ramp compensation.

2 switch−Forward Power supply specification:

- Regulated output: 12V
- L_{out}=27μH
- V_f=0.7V
- Current sense resistor: 0.75Ω
- Switching frequency: 100kHz
- V_{bulk}=350V, minimum input voltage at which the power supply works.
- Duty cycle max: DCmax =75%
- V_{ramp}=3.5V, Internal ramp level.
- R_{ramp}=26.5kΩ, Internal pull−up resistance
- Targeted ramp compensation level: 100%
- Transformer specification: L_{mag}=8mH, N_s/N_p=0.085

Secondary−side downslope projected over the sense resistor is:

$$S_{CS}=\frac{(V_{out}+V_f)}{L_{out}}\frac{N_s}{N_p}R_{CS} \Rightarrow S_{CS}=\frac{(12+0.7)}{27\bullet10^{-6}}0.085\times0.75=30\text{mV/μS}$$

The natural primary ramp is:

$$S_{natural}=\frac{V_{bulk}}{L_{mag}}R_{CS} \Rightarrow S_{natural}=\frac{350}{8*10^{-3}}0.75=32.8\text{mV/μS}$$

And the natural ramp compensation will be:

$$\delta_{natural\_comp}=\frac{S_{natural}}{S_{CS}} \Rightarrow \delta_{natural\_comp}=\frac{32.8}{30}\approx110\%$$

So in that case the natural ramp compensation due to the magnetizing inductance of the transformer will be enough to prevent any sub−harmonics oscillation in case of duty cycle above 50%.

■ TYPICAL APPLICATION CIRCUIT