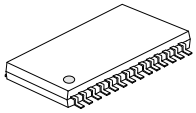
STEREO AUDIO PROCESSOR FOR CAR AUDIO



SOP-28

■ DESCRIPTION

The **UAP7313** is an audio processor, includes 3 stereo input selector with adjustable gain, master volume control with low frequency loudness compensation, individual output attenuator and tone control. designed for versatile application. It is a good solution for the car audio signal processing.

Due to the high reliability requirement from the car audio business, the **UAP7313** improves both audio performances and input surge current capability, these causes the **UAP7313** is the best solution for the cost-effective car audio systems.

■ FEATURES

* 3 stereo inputs with gain selection, range from 0dB to +11.25dB in 3.75dB/step
* Master volume from 0 dB to -78.75dB in 1.25dB/step
* Speaker attenuator for balance and fader, range from 0dB to -38.75dB in 1.25dB/step
* Each channel output can be muted individually.
* Bass and Treble control, range from -14dB to +14dB in 2dB/step
* Wide operation range (V_{DD} = 4V to 10V)

■ TYPICAL APPLICATIONS

* Car Audio
* Home Audio System
* Powered Speaker System

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UAP7313L-S28-R	UAP7313G-S28-R	SOP-28	Tape Reel

UAP7313G-S28-R
- (1)Packing Type
- (2)Package Type
- (3)Green Package

(1) R: Tape Reel
(2) S28: SOP-28
(3) G: Halogen Free and Lead Free, L: Lead Free

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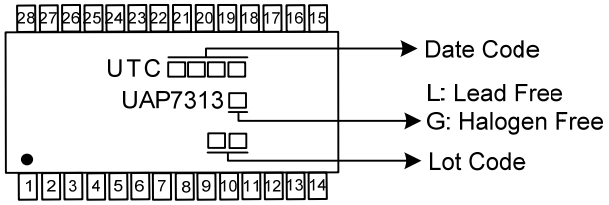
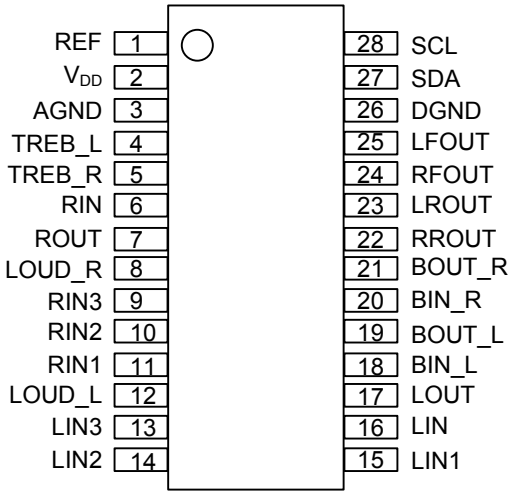
■ MARKING



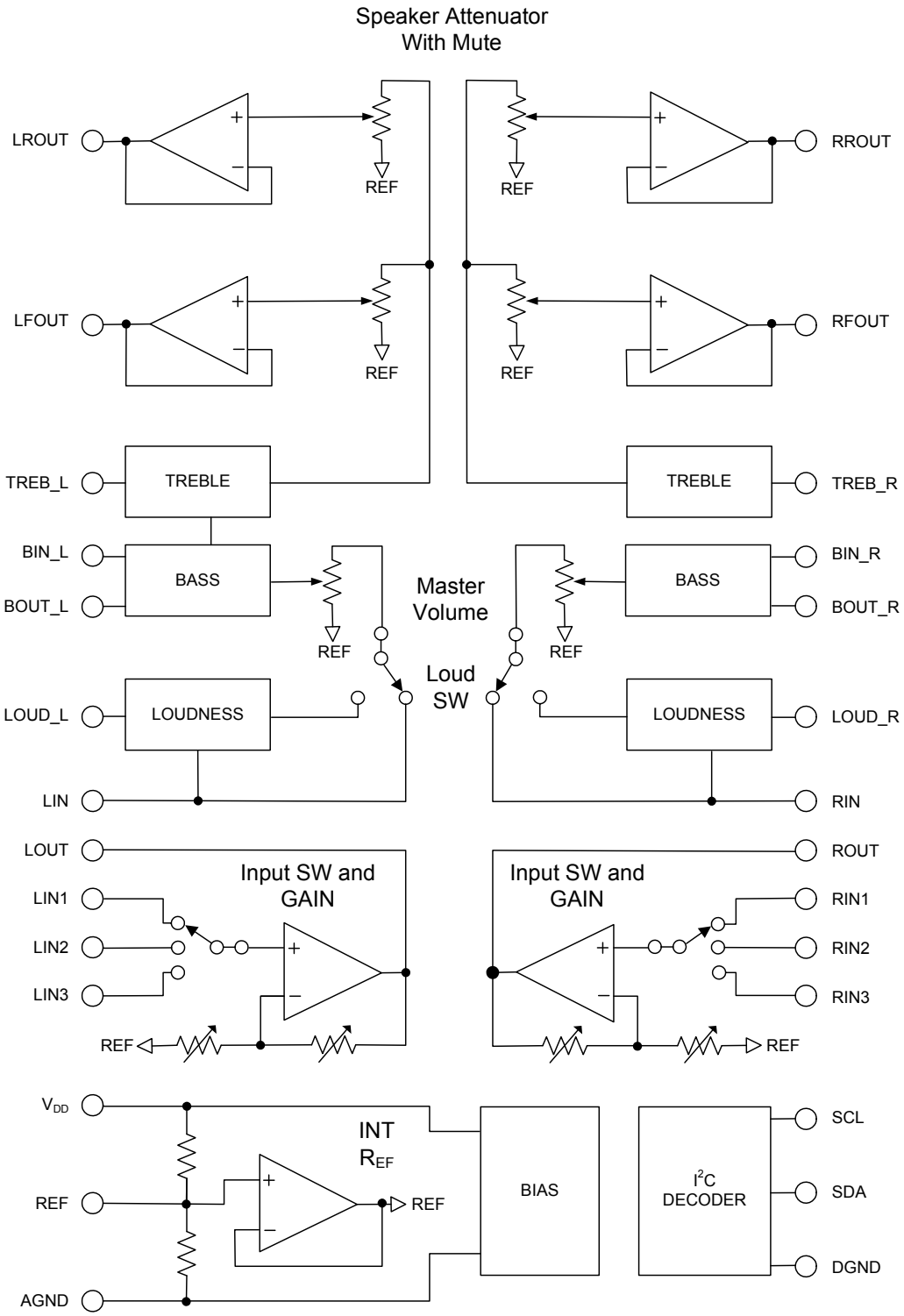
■ PIN CONFIGURATIONS



■ PIN DESCRIPTION

PIN No.	PIN NAME	I/O	Description
1	REF	-	Analog reference voltage ($1/2V_{DD}$)
2	V_{DD}	-	Supply input voltage
3	AGND	-	Analog ground
4/5	TREB_L/R	I	Left/Right channel input for treble controller
6	RIN	I	Right channel volume controller input
7	ROUT	O	Right channel Input selector output
8	LOUD_R	I	Right channel loudness input
9/10/11	RIN3/2/1	I	Right channel input 3/2/1
12	LOUD_L	I	Left channel loudness input
13/14/15	LIN3/2/1	I	Left channel input 3/2/1
16	LIN	I	Left channel volume controller input
17	LOUT	O	Left channel Input selector output
18	BIN_L	I	Left channel input for bass controller
19	BOUT_L	O	Left channel output for bass controller
20	BIN_R	I	Right channel input for bass controller
21	BOUT_R	O	Right channel output for bass controller
22	RROUT	O	Right rear speaker output
23	LROUT	O	Left rear speaker output
24	RFOUT	O	Right front speaker output
25	LFOUT	O	Left front speaker output
26	DGND	-	Digital ground
27	SDA	I	I^2C data input
28	SCL	I	I^2C clock input

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Operating Supply Voltage	V_{DD}	-0.3 ~ 10	V
Input Voltage	V_{IN}	-0.3 ~ V_{DD}+0.3	V
Operating Temperature	T_{OPR}	-40 ~ +85	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ TYPICIAL WORKING SUITATION

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply V_{DD} voltage	V_{DD}	4	9	10	V
Max input signal handling	V_{CL}	2.3	2.6		Vrms
Total harmonic distortion (1Vrms,1KHz)	THD		0.03	0.07	%
Signal To noise ratio	S/N		100		dBV
Channel separation (f=1KHz)	S_C		100		dB
Volume control 1.25dB step	A_{U_Volume}	-78.75		0	dB
Bass & treble control 2dB step	$A_{U\_Bass\ \&\ Treble}$	-14		+14	dB
Balance control 1.25dB step	$A_{U\_Speaker}$	-37.5		0	dB
Input gain 3.75dB step	A_{U_Gain}	0		11.25	dB
Mute attenuation	A_{U_Mute}		100		dB

■ ELECTRICAL CHARACTERISTICS

(V_{DD}=9V, R_L=100KΩ, R_G=20Ω, all controls flat, F=1KHz, and all of peripheral components according to standard application circuit. T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
Supply Voltage	V_{DD}		5	9	10	V
Supply Current	I_S	V_{DD}=9V		30	40	mA
		V_{DD}=5V		25	32	mA
INPUT SELECTORS						
Input Resistance	R_{IN}	Input 1,2,3		50		KΩ
Maximum Input Level	V_{I_MAX}	All Gain=0dB, THD=1%	2.3	2.6		V_{rms}
Input Separation	IS_{IN}	F=20~20KHz		100		dB
Maximum Input Gain	G_{IN_MIN}		-1	0	1	dB
Maximum Input Gain	G_{IN_MAX}		10.5	11.25	12	dB
Step Resolution	G_{INst}			3.75		dB
Gain Set Error	E_A		-1	0	1	dB
Minimum Load	R_L	V_O=2 V_{rms}, L_{OUT}, R_{OUT}	5			KΩ
DC Offset	V_{DCO}	0dB~+11.25dB		3	10	mV
VOLUME CONTROL						
Input Resistance	R_{IN}	V_{OL}=0dB		20		KΩ
Maximum Attenuation	A_{VMIN}		-1	0	1	dB
Maximum Attenuation	A_{VMAX}		-75	-78.75	-82	dB
Step Resolution	A_{STEP}		1.15	1.25	1.3	dB
Attenuation Set Error	E_A	V_{OL}=0~-70dB	-1	0	1	dB
SPEAKER ATTENUATORS						
Maximum Gain	A_{VMIN}		-1	0	1	dB
Maximum Attenuation	A_{VMAX}		-36	-38.75	-39	dB
Step Resolution	S_{STEP}		1.15	1.25	1.35	dB
Attenuation Set Error	E_A		-1	0	1	dB
Output Mute Attenuation	A_{MUTE}			100		dB
DC Offset	V_{DCO}	0dB to MUTE		5	10	mV

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BASS CONTROL						
Control Range	G_b	Max Boost/Cut	±12	±14	±16	dB
Step Resolution	S_{STEP}		1.7	2.0	2.2	dB
Feedback Resistance	R_B			44		KΩ
TREBLE CONTROL						
Control Range	G_t	Max Boost/cut	±12	±14	±16	dB
Step Resolution	T_{STEP}		1.7	2	2.3	dB
LOUDNESS CONTROL						
Boost Gain	G_{LD}	Volume=-40dB, F=20Hz	18	20	22	dB
AUDIO OUTPUT						
Maximum Output Level	V_{OMAX}	THD=1%	2.3	2.6		V_{rms}
DC Voltage Level	V_{OUT}		0.49	0.5	0.51	V_{DD}
Minimum Load	R_L		5			KΩ
GENERAL						
Signal to Noise Ratio	SNR	All Gain=0dB, A-weighted		100		dBV
		All Gain=0dB, Muted		100		dBV
Distortion	THD	All Gain=0dB, V_{IN} =1Vrms		0.03	0.07	%
		All Gain=0dB, V_{IN}=100mVrms		0.01	0.03	%
Channel Separation	Cs	L to R or R to L channel		100		dB
I^2C Crosstalk	Ct	I^2C to audio output		90		dB
Ripple Rejection	PSRR	C_{REF}=22μF, F=100Hz		75		dB
I^2C BUS						
Input Low Voltage	V_{IL}	V_{DD}=9V			1	V
Input High Voltage	V_{IH}	V_{DD}=9V	3			V
Input Current	I_{IN}		-5		+5	uA
SDA Pull Down Voltage	V_{ACK}	Rpull up=3K, ACK=active		0.4		V

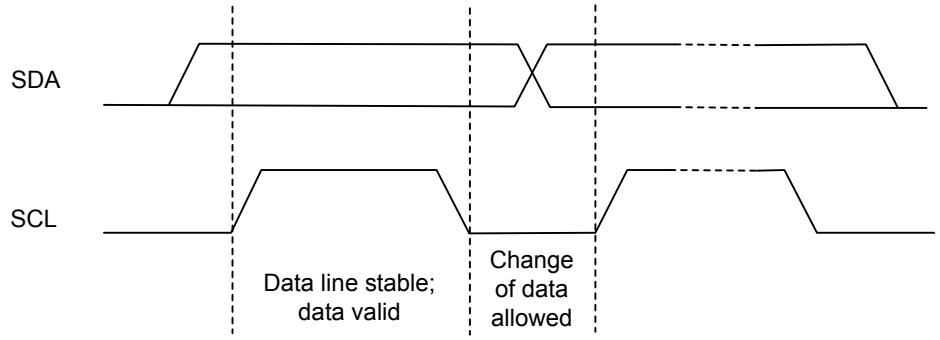
■ FUNCTIONAL DESCRIPTION

Bus Interface

All functions of the **UAP7313** are controlled by the I^2C interface, the interface is consisting by SDA and SCL pins. Detail protocol of the I^2C bus will discuss on the next section. It should be noted that the bus level pull-up resistors connected to the **UAP7313** positive supply voltage may required in some application especially the MCU output high level is no enough.

Data Validity

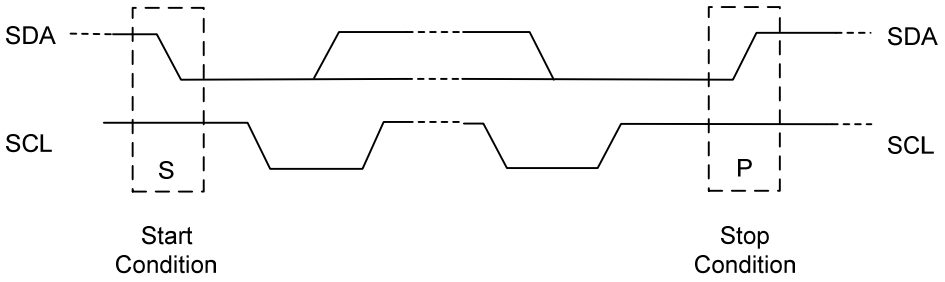
A data on the SDA Line is considered valid and stable only w hen the SCL Signal is in HIGH State. The HIGH and LOW State of the SDA Line can only change when the SCL signal is LOW.



Start And Stop Conditions

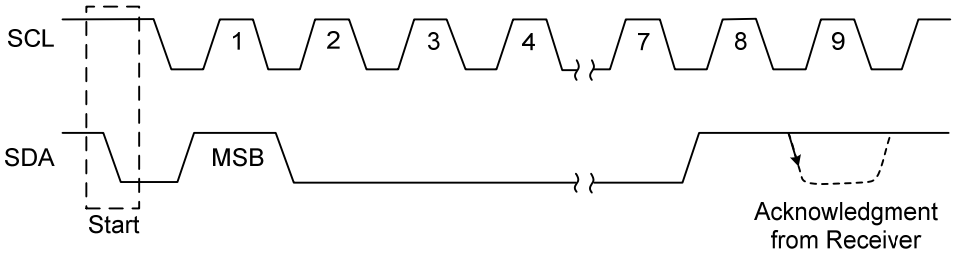
A Start Condition is activated when SCL is set to HIGH and SDA shifts from HIGH to LOW State.

The Stop Condition is activated when SCL is set to HIGH and SDA shifts from LOW to HIGH State.



Acknowledge

During the Acknowledge clock pulse (ACK), the SDA output port of the master device (μP) would be sets on Hi-Z state, if peripheral device (ex : audio processor) recognize the I^2C command the SDA line will be pull-down by slave device during the SCL clock pulse held in HIGH state period. The slave device that has been addressed to generate an Acknowledge after receiving each byte, otherwise, the SDA Line will remain at the High level in period of the ninth (9th) clock pulse. In this case, the host controller will generate a STOP sign in order to abort the transfer mission.



■ FUNCTIONAL DESCRIPTION (Cont.)

Interface Protocol

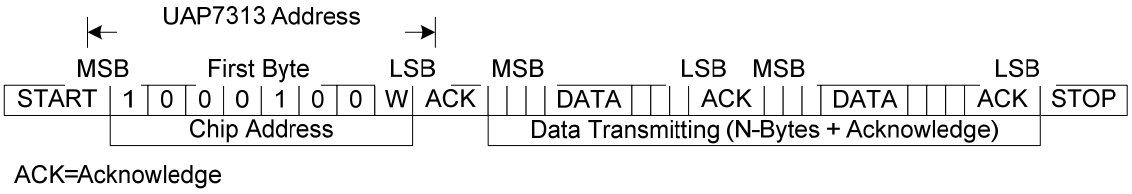
The interface protocol sequence was defined in beLow section:

A Start sign

A Chip Address of the desire slave device. The W Bit must be “0” (written). The **UAP7313** will always response an Acknowledge on the end of each byte.

A Data Sequence (N-Bytes + Acknowledge)

A Stop Condition



ACK=Acknowledge

I²C Bus Initial Time

The **UAP7313** is controlled by the I2C bus command; each time the supply voltage applied to chip it needs an initial time to reset all of the internal decoder register, in this period access the I²C bus is prohibited. The initial time is determinate by capacitance it attached on REF pin (C_{REF}) and Td. For proper operation USER must check the I²C starts timing is fit this requirement and recommended Td timing shown on next page is 50mS.

Data Bytes

MSB							LSB	FUNCTION
0	0	B2	B1	B0	A2	A1	A0	Master Volume
1	1	0	B1	B0	A2	A1	A0	Speaker ATT LR
1	1	1	B1	B0	A2	A1	A0	Speaker ATT RR
1	0	0	B1	B0	A2	A1	A0	Speaker ATT LF
1	0	1	B1	B0	A2	A1	A0	Speaker ATT RF
0	1	0	G1	G0	LD	S1	S0	Input Switch and Gain
0	1	1	0	C3	C2	C1	C0	Bass Control
0	1	1	1	C3	C2	C1	C0	Treble Control

■ FUNCTIONAL DESCRIPTION (Cont.)

Input Selector

MSB							LSB	FUNCTION
0	1	0	G1	G0	LD	S1	S0	Audio switch
						0	0	Stereo 1
						0	1	Stereo 2
						1	0	Stereo 3
					0			Loudness ON
					1			Loudness OFF
			0	0				+11.25dB
			0	1				+7.5dB
			1	0				+3.75dB
			1	1				0dB

Master Volume

MSB							LSB	FUNCTION
0	0	B2	B1	B0	A2	A1	A0	1.25dB step
					0	0	0	0dB
					0	0	1	-1.25dB
					0	1	0	-2.5dB
					0	1	1	-3.75dB
					1	0	0	-5dB
					1	0	1	-6.25dB
					1	1	0	-7.5dB
					1	1	1	-8.75dB
0	0	B2	B1	B0	A2	A1	A0	10dB step
		0	0	0				-dB
		0	0	1				-10dB
		0	1	0				-20dB
		0	1	1				-30dB
		1	0	0				-40dB
		1	0	1				-50dB
		1	1	0				-60dB
		1	1	1				-70dB

■ FUNCTIONAL DESCRIPTION (Cont.)

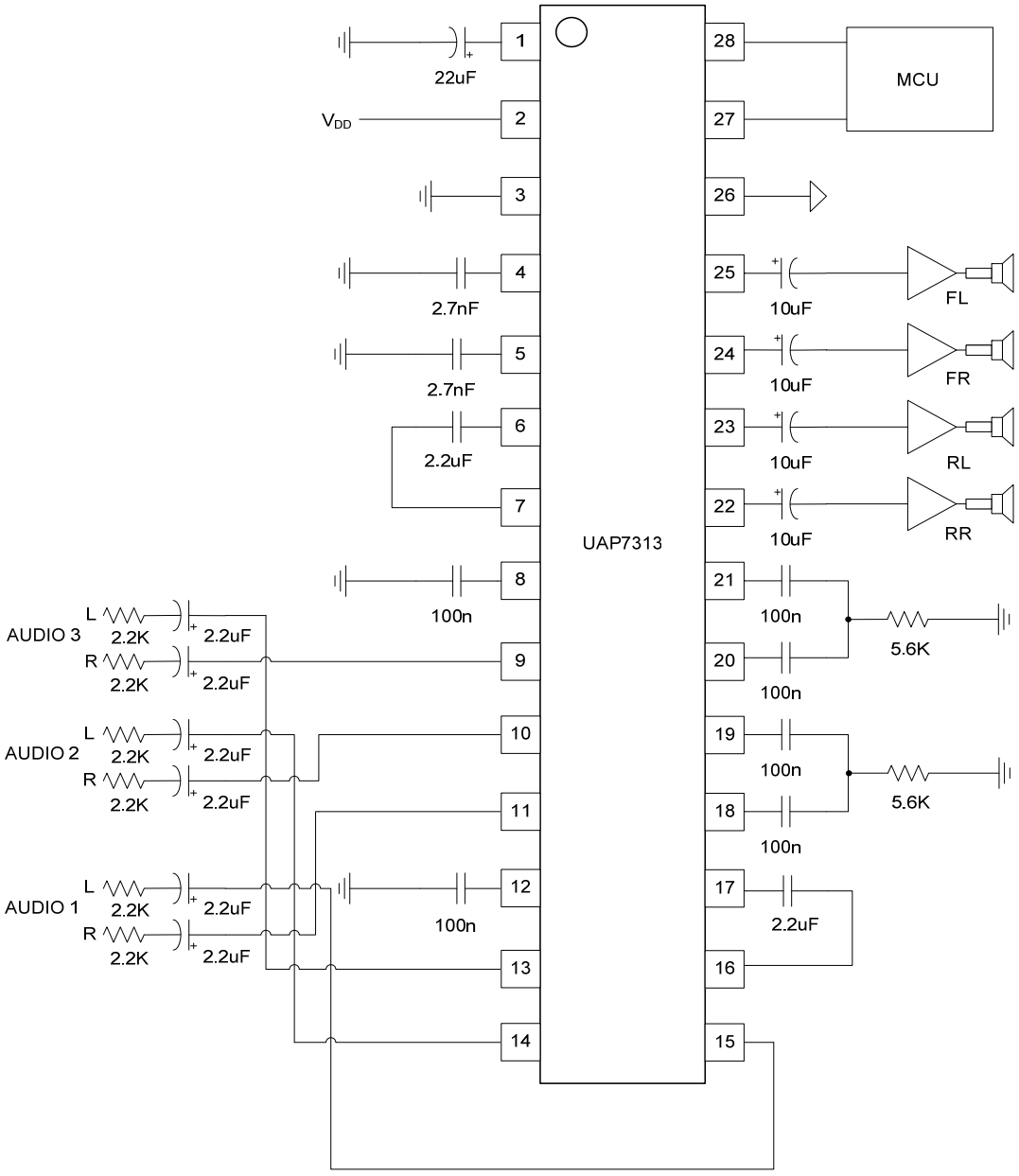
Bass And Treble Data Bytes

MSB							LSB	FUNCTION
0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Treble
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				0	0	1	0	-10dB
				0	0	1	1	-8dB
				0	1	0	0	-6dB
				0	1	0	1	-4dB
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	1	1	1	0dB
				1	1	1	0	+2dB
				1	1	0	1	+4dB
				1	1	0	0	+6dB
				1	0	1	1	+8dB
				1	0	1	0	+10dB
				1	0	0	1	+12dB
				1	0	0	0	+14dB

Speaker Attenuators

MSB							LSB	FUNCTION
1	0	0	B1	B0	A2	A1	A0	Speaker LF
1	0	1	B1	B0	A2	A1	A0	Speaker RF
1	1	0	B1	B0	A2	A1	A0	Speaker LR
1	1	1	B1	B0	A2	A1	A0	Speaker RR
					0	0	0	0dB
					0	0	1	-1.25dB
					0	1	0	-2.5dB
					0	1	1	-3.75dB
					1	0	0	-5dB
					1	0	1	-6.25dB
					1	1	0	-7.5dB
					1	1	1	-8.75dB
			0	0				0dB
			0	1				-10dB
			1	0				-20dB
			1	1				-30dB
			1	1	1	1	1	Mute

■ TYPICAL APPLICATION CIRCUIT



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