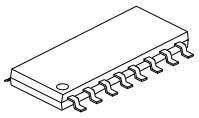
FET BIAS CONTROLLER



SOP-16

■ DESCRIPTION

The UTC **L4002** is specially designed integrated circuit for 2.5V satellite receiver front-end block. It provides stable drain and gate bias conditions for GaAs or HEMT FETs.

The UTC **L4002** provides four FETs bias control respectively. By adjusting an internal resistors, it can change the FET's bias current to optimize the satellite receiver front end block performances.

It generates the required negative voltage to bias the gate of GaAs FET, and internally provides protection circuit that can protect the FET devices during supply voltage transient. So it is very popular in satellite receiver front end block.

■ FEATURES

* Built in FET device protection circuit
* Stable bias control for GaAs and HEMT FETs
* Drive up to four FETs
* 2.5V supply voltage

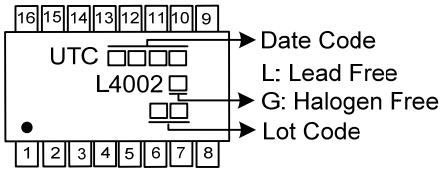
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
L4002L-S16-R	L4002G-S16-R	SOP-16	Tape Reel

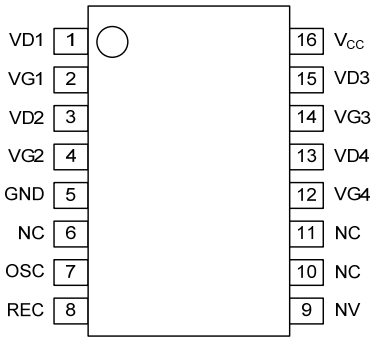
L4002G-S16-R
(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) S16: SOP-16
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



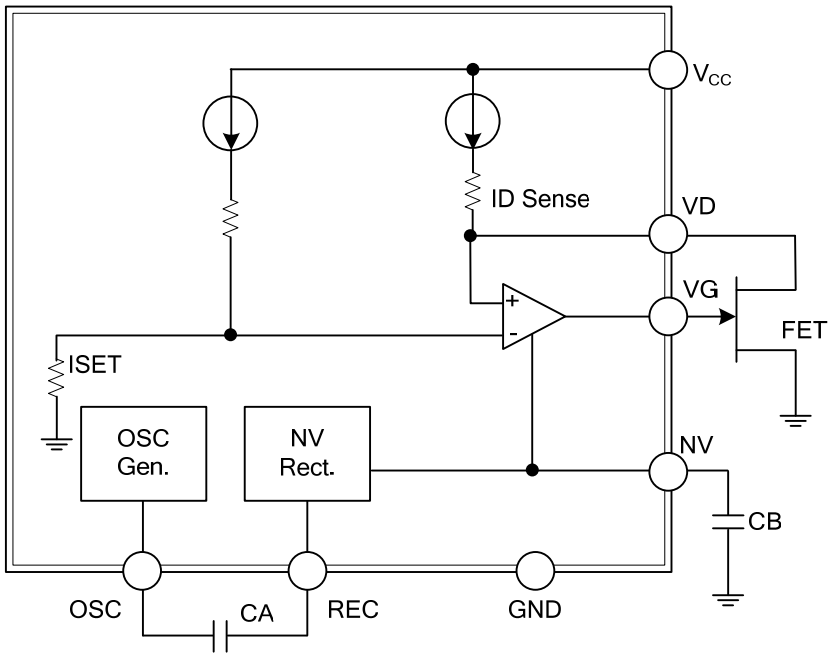
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	VD1	1st Drain output voltage
2	VG1	1st Gate output voltage
3	VD2	2nd Drain output voltage
4	VG2	2nd Gate output voltage
5	GND	Ground
6	NC	No connect
7	OSC	OSC output
8	REC	Rectifier Input
9	NV	Negative voltage output
10	NC	No connect
11	NC	No connect
12	VG4	4th Gate output voltage
13	VD4	4th Drain output voltage
14	VG3	3rd Gate output voltage
15	VD3	3rd Drain output voltage
16	V_{CC}	Supply voltage

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.6~3	V
Supply Current	I_{CC}	100	mA
Maximum Drain Current	I_D	15	mA
Maximum CSUB Sink Current	I_{CSUB}	-500	μA
Operating Temperature	T_{OPR}	-40 ~ +85	°C
Storage Temperature	T_{STG}	-50 ~ +125	°C

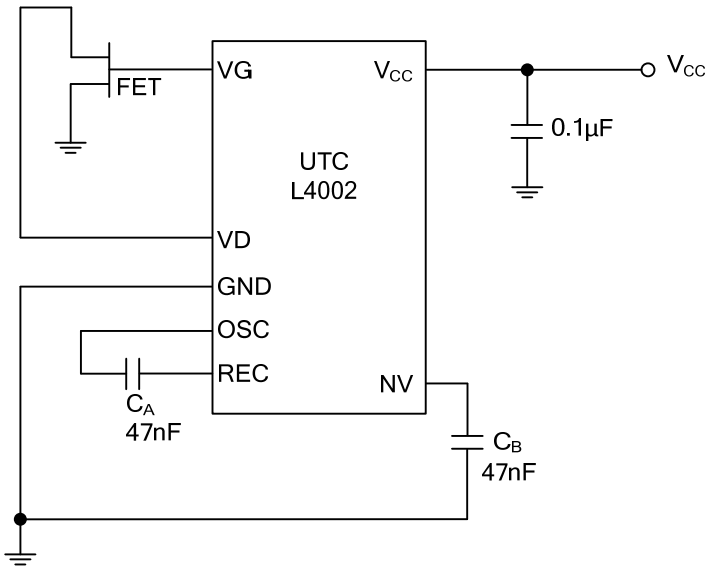
Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS

(V_{CC}=2.5V, I_D=9.5mA, T_A=25°C, unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.375	2.5	2.625	V
Supply Current	I_{CC}	No FET		6	10	mA
Negative Voltage	V_{NV}	I_{NV}=0uA, V_{CC}=2.5V		-2	-1	V
		I_{NV}=-200uA			-1	V
Oscillator Freq.	f_O		300	600	800	KHz
Drain Current	I_D		8	9.5	12	mA
Drain Current Change with V_{CC}	ΔI_{DV}	V_{CC}=2.375V~2.625V		2		%/V
VD1/VD2/VD3/VD4 Drain Offset Current	ΔI_{DC}			0.5		mA
Drain Current Change with Temp.	ΔI_{DT}	T=-40~85°C		0.5		%/°C
Drain Voltage	V_D	I_D=9.5mA	1.8	2	2.2	V
Drain Voltage Change with V_{CC}	ΔV_{DV}	V_{CC}=2.375V~2.625V		0.5		%/V
Drain Voltage Change	ΔV_{DT}	T=-40~85°C		100		ppm/°C
Dynamic Gate Voltage Range	V_G	NV without loading	-2		0.7	V
Drain Output Noise Voltage	V_{dn}	With Drain bypass capacitor=10nF			0.05	V_{PP}
Gate Output Noise Voltage	V_{GN}	With Gate bypass capacitor=10nF			0.03	V_{PP}

■ TYPICAL APPLICATION CIRCUIT



There are three major functions provided by UTC **L4002**: support negative voltage, bias control circuit, and FET protecting circuit.

The negative voltage is generated using internal oscillator. It only needs an ac coupled capacitor C_A 47nF and a negative voltage bypass capacitor C_B 47nF.

The UTC **L4002** devices have been designed to protect the external FETs from adverse operating conditions. With a JFET connected to any bias circuit, the gate output voltage of the bias circuit can not exceed the range -2V to 0.7V, under any conditions including powerup and powerdown transients. Should the negative bias generator be shorted or overloaded so that the drain current of the external FETs can no longer be controlled, the drain supply to FETs is shut down to avoid damage to the FETs by excessive drain current. The following diagrams show the UTC **L4002** in typical LNB applications. Within each FET gain stage the numbering system indicates how the bias stages relate to the application circuits.