



U74LVC2G02

CMOS IC

DUAL 2-INPUT POSITIVE-NOR GATE

DESCRIPTION

The UTC **U74LVC2G02** is a dual 2-input positive-NOR gate which provides the function $Y=\overline{A+B}$ or $Y=\overline{A+\overline{B}}$.

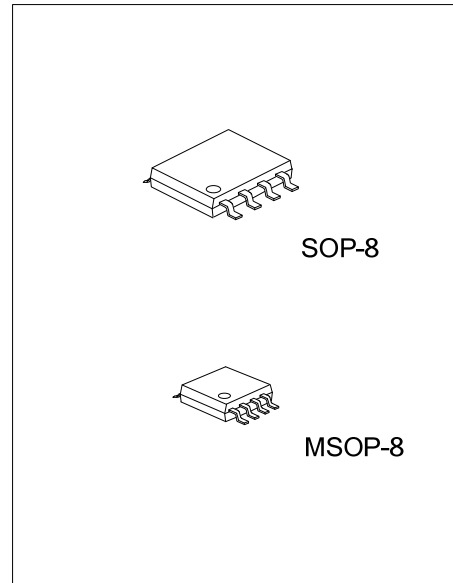
This device has power-down protective circuit, preventing device destruction when it is powered down.

FEATURES

- * Operation Voltage Range: 1.65~5.5V
- * Low Power Dissipation: $I_{CC}=10\mu A(\text{Max.})$
- * High Speed: $t_{PD}=4.9ns(V_{CC}=3.3V)$
- * Specified from -40 to +85°C

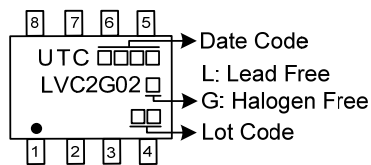
ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC2G02L-S08-R	U74LVC2G02G-S08-R	SOP-8	Tape Reel
U74LVC2G02L-SM1-R	U74LVC2G02G-SM1-R	MSOP-8	Tape Reel

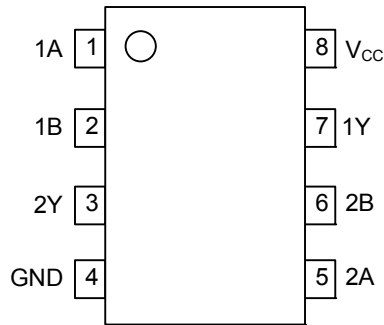


<p>U74LVC2G02G-S08-R</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) R: Tape Reel (2) S08: SOP-8, SM1: MSOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



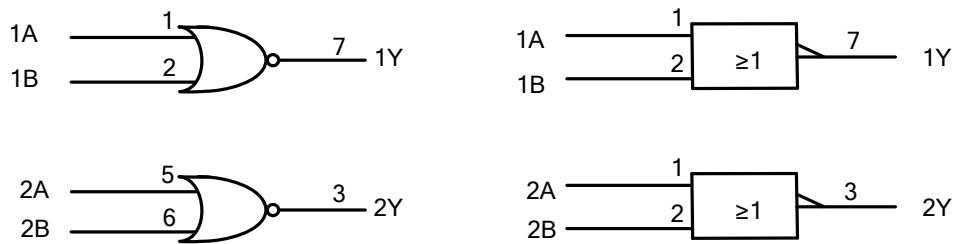
■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

■ LOGIC DIAGRAM (positive logic)



IEC logic symbol

■ ABSOLUTE MAXIMUM RATINGS (T_A =25°C , unless otherwise specified) (Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{CC}	-0.5 ~ 6.5	V
Input Voltage	V _{IN}	-0.5 ~ 6.5	V
Output Voltage	V _{OUT}	-0.5 ~ V _{CC} +0.5	V
Input Clamp Current	I _{IK}	-50	mA
Output Clamp Current	I _{OK}	-50	mA
Output Current	I _{OUT}	±50	mA
V _{CC} or GND Current	I _{CC}	±100	mA
Storage Temperature	T _{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V _{CC}		1.65	3.3	5.5	V
Input Voltage	V _{IN}		0		5.5	V
Output Voltage	V _{OUT}		0		V _{CC}	V
Input Transition Rise or Fall rate	Δ t/ΔV	V _{CC} =1.8V±0.15V, 2.5V±0.2V			20	ns/V
		V _{CC} =3.3V±0.3V			10	
		V _{CC} =5V±0.5V			5	
Operating Temperature	T _A		-40		+125	°C

■ STATIC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V _{IH}	V _{CC} =1.65V~1.95V	0.65×V _{CC}			V
		V _{CC} =2.3V~2.7V	1.7			
		V _{CC} =3V~3.6V	2			
		V _{CC} =4.5V~5.5V	0.7×V _{CC}			
Low-Level Input Voltage	V _{IL}	V _{CC} =1.65V~1.95V			0.35×V _{CC}	V
		V _{CC} =2.3V~2.7V			0.7	
		V _{CC} =3V~3.6V			0.8	
		V _{CC} =4.5V~5.5V			0.3×V _{CC}	
High-Level Output Voltage	V _{OH}	V _{CC} =1.65~5.5V, I _{OH} =-100μA	V _{CC} -0.1			V
		V _{CC} =1.65V, I _{OH} =-4mA	1.2			
		V _{CC} =2.3V, I _{OH} =-8mA	1.9			
		V _{CC} =3V, I _{OH} =-16mA	2.4			
		V _{CC} =3V, I _{OH} =-24mA	2.3			
		V _{CC} =4.5V, I _{OH} =-32mA	3.8			
Low-Level Output Voltage	V _{OL}	V _{CC} =1.65~5.5V, I _{OL} =100μA			0.1	V
		V _{CC} =1.65V, I _{OL} =4mA			0.45	
		V _{CC} =2.3V, I _{OL} =8mA			0.3	
		V _{CC} =3V, I _{OL} =16mA			0.4	
		V _{CC} =3V, I _{OL} =24mA			0.55	
		V _{CC} =4.5V, I _{OL} =32mA			0.55	
Input Leakage Current	I _{I(LEAK)}	V _{CC} =0 to 5.5V, V _{IN} =5.5V or GND			±5	μA
Power off Current	I _{off}	V _{CC} =0V, V _{IN} or V _{OUT} =5.5V			±10	μA

■ STATIC CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Quiescent Supply Current		$V_{CC}=1.65\sim 5.5V$, $V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$			10	μA
Additional Quiescent Supply Current Per Input Pin	ΔI_{CC}	$V_{CC}=3\sim 5.5V$, One input at $V_{CC}-0.6V$, Other inputs at V_{CC} or GND			500	μA
Input Capacitance	C_{IN}	$V_{CC}=3.3V$, $V_{IN}=V_{CC}$ or GND		5		pF

■ DYNAMIC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay From Input (A or B) to Output(Y)	t_{PHL} / t_{PLH}	$V_{CC} = 1.8V \pm 0.15V$, $C_L = 30$ pF, $R_L = 1K\Omega$	3.2		8.9	ns
		$V_{CC} = 2.5V \pm 0.2V$, $C_L = 30$ pF, $R_L = 500\Omega$	1.0		5.4	
		$V_{CC} = 3.3V \pm 0.3V$, $C_L = 50$ pF, $R_L = 500\Omega$	1.0		4.9	
		$V_{CC} = 5V \pm 0.5V$, $C_L = 50$ pF, $R_L = 500\Omega$	1.0		4.4	

Note: See Fig. 1 and Fig. 2 for test circuit and waveforms.

■ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Cpd Power Dissipation Capacitance	C_{PD}	$V_{CC}=3.3V$, $f=10MHz$		19		pF

■ TEST CIRCUIT AND WAVEFORMS

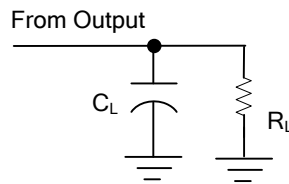


Fig.1 TEST CIRCUIT

V _{CC}	Inputs		V _M	C _L	R _L
	V _{IN}	t _r , t _f			
1.8V±0.15V	V _{CC}	≤2ns	V _{CC} /2	30pF	1KΩ
2.5V±0.2V	V _{CC}	≤2ns	V _{CC} /2	30pF	500Ω
3.3V±0.3V	3V	≤2.5ns	1.5V	50pF	500Ω
5V±0.5V	V _{CC}	≤2.5ns	V _{CC} /2	50pF	500Ω

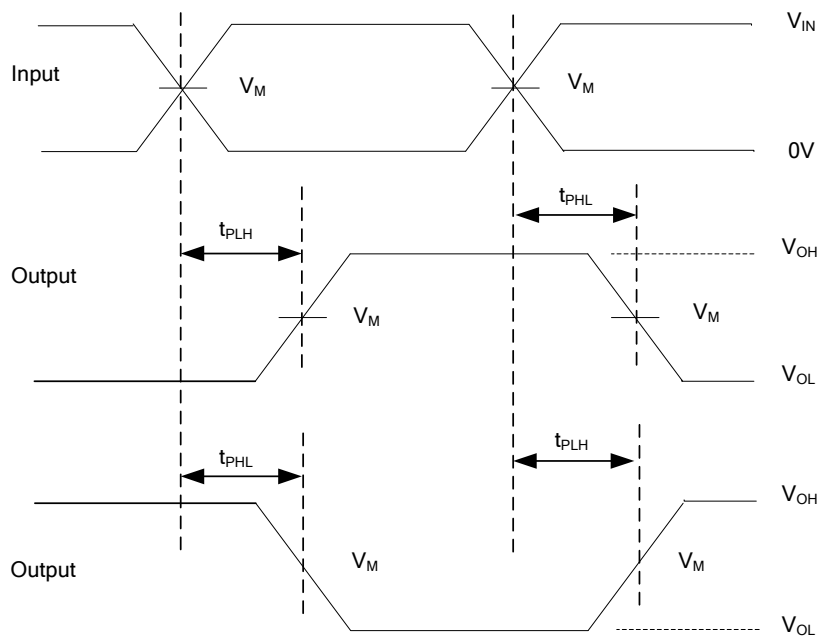


Fig.2 PROPAGATION DELAY TIMES

Note: C_L includes probe and jig capacitance.

All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Zo = 50Ω.

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