



UTT21NN03

Power MOSFET

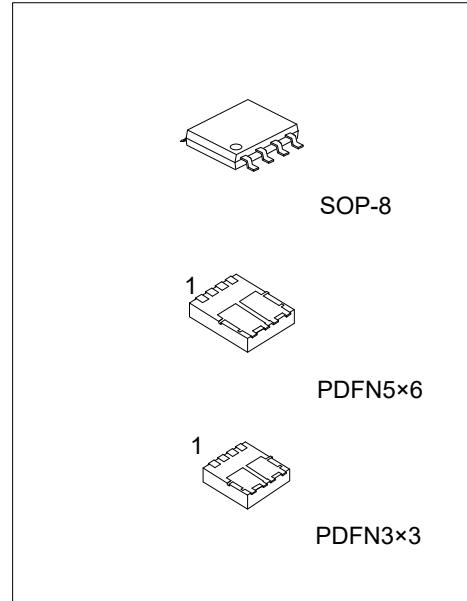
21A, 30V DUAL N-CHANNEL ENHANCEMENT MODE POWER MOSFET

■ DESCRIPTION

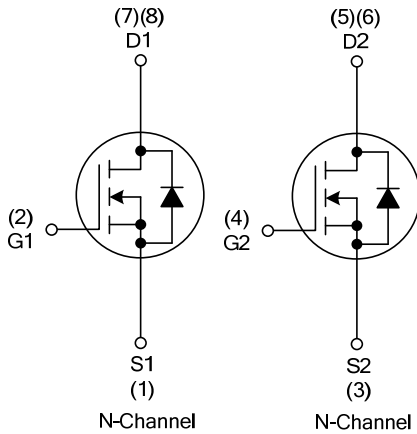
The UTC **UTT21NN03** is a N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with low $R_{DS(ON)}$ characteristic by high cell density trench technology.

■ FEATURES

- * $R_{DS(ON)} \leq 23\text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=10.5\text{A}$
- $R_{DS(ON)} \leq 35\text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$, $I_D=10.5\text{A}$
- * Fast Switching Speed
- * Simple Drive Requirement



■ SYMBOL



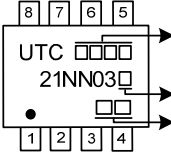
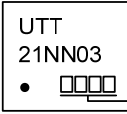
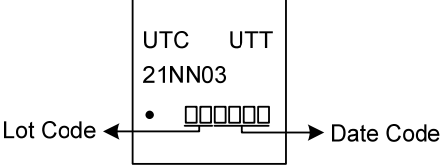
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UTT21NN03L-S08-R	UTT21NN03G-S08-R	SOP-8	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel
UTT21NN03L-P3030-R	UTT21NN03G-P3030-R	PDFN3x3	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel
UTT21NN03L-P5060-R	UTT21NN03G-P5060-R	PDFN5x6	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UTT21NN03G-S08-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) S08: SOP-8, P3030: PDFN3x3, P5060: PDFN5x6</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING

Package	MARKING
SOP-8	 <p> UTC □□□□ → Date Code L: Lead Free G: Halogen Free □□□□ → Lot Code </p>
PDFN3x3	 <p> UTT 21NN03 • □□□□ → Date Code </p>
PDFN5x6	 <p> UTC UTT 21NN03 • □□□□□□ → Date Code Lot Code ← □□□□□□ </p>

■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V _{DSS}	30	V
Gate-Source Voltage		V _{GSS}	±20	V
Drain Current	Continuous	SOP-8	8.5	A
		PDFN5X6 PDFN3X3	10.5	A
	Pulsed (Note 2)	I _{DM}	21	A
Avalanche Energy	Single Pulsed (Note 3)	E _{AS}	4.5	mJ
Power Dissipation	SOP-8	P _D	1.2	W
	PDFN3×3		1.66	W
	PDFN5×6		1.92	W
Junction Temperature		T _J	+150	°C
Storage Temperature		T _{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. L=0.5mH, I_{AS}=4.2A, V_{DD}=30V, R_G = 25Ω, Starting T_J = 25°C

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-8	θ _{JA}	125	°C/W
	PDFN3×3		75	°C/W
	PDFN5×6		65	°C/W
Junction to Case	SOP-8	θ _{JC}	104	°C/W
	PDFN3×3		7.8	°C/W
	PDFN5×6		6.9	°C/W

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

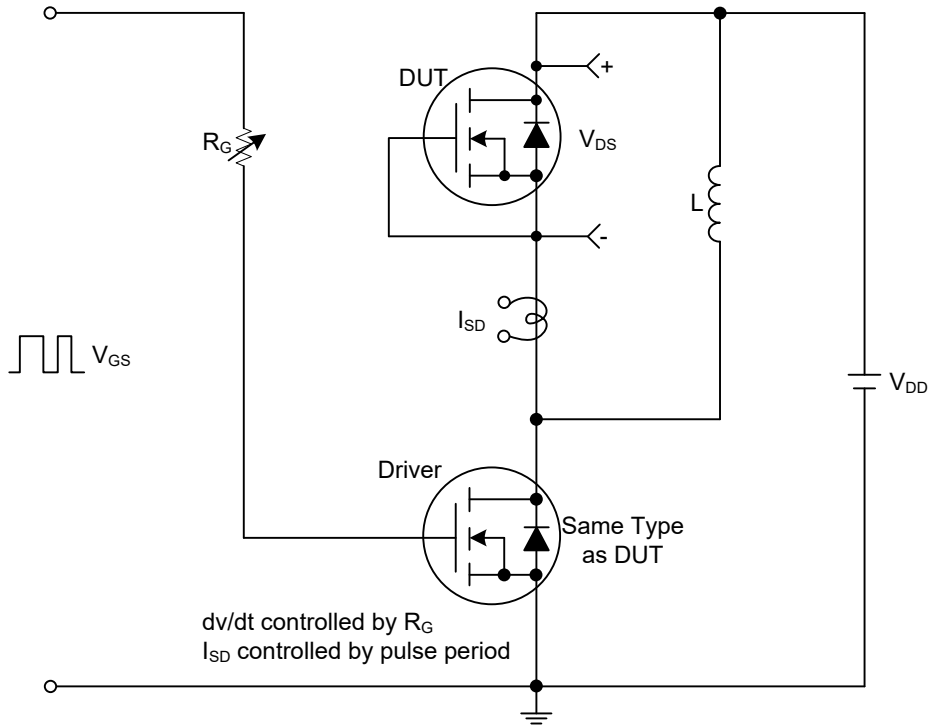
■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	30			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	V _{DS} =0V, V _{GS} =20V			100	nA
	Reverse		V _{DS} =0V, V _{GS} =-20V			-100
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	V
Drain-Source On-State Resistance	R _{DSON}	V _{GS} =10V, I _D =10.5A			23	mΩ
		V _{GS} =4.5V, I _D =10.5A			35	mΩ
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		394		pF
Output Capacitance	C _{OSS}			85		pF
Reverse Transfer Capacitance	C _{RSS}			71		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q _G	V _{DS} =30V, V _{GS} =10V, I _D =10A, (Note 1, 2)		13		nC
Gate-Source Charge	Q _{GS}			1.8		nC
Gate-Drain Charge	Q _{GD}			2.4		nC
Turn-ON Delay Time (Note 1)	t _{D(ON)}	V _{DD} =30V, V _{GS} =10V, I _D =10A, R _G =25Ω (Note 1, 2)		7		ns
Turn-ON Rise Time	t _R			15		ns
Turn-OFF Delay Time	t _{D(OFF)}			39		ns
Turn-OFF Fall Time	t _F			32		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I _S				10.5	A
Maximum Body-Diode Pulsed Current	I _{SM}				21	A
Drain-Source Diode Forward Voltage (Note 1)	V _{SD}	I _S =21A, V _{GS} =0V			1.3	V

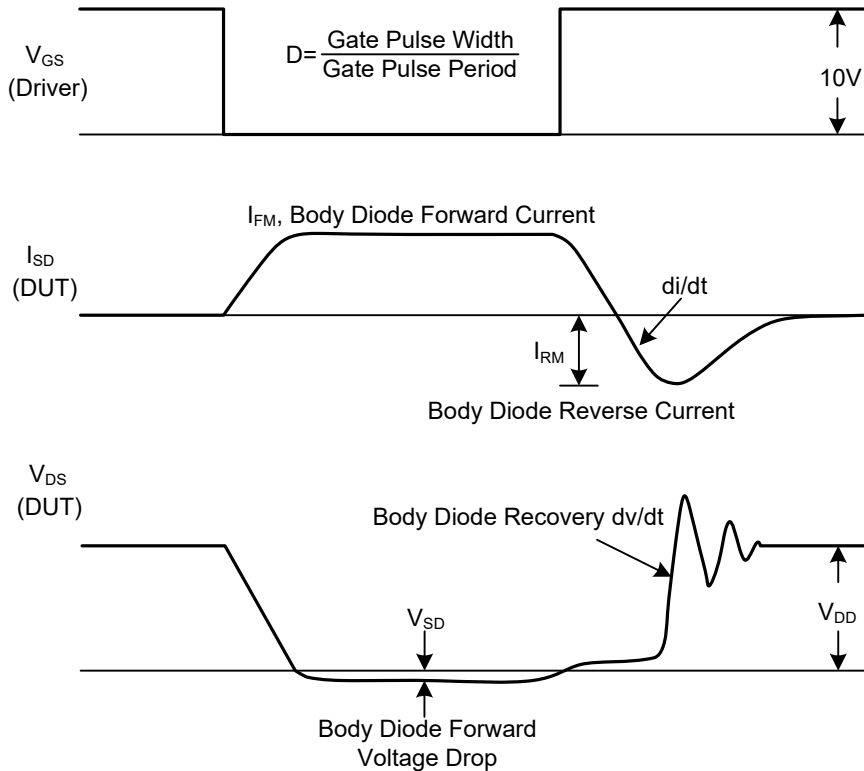
Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



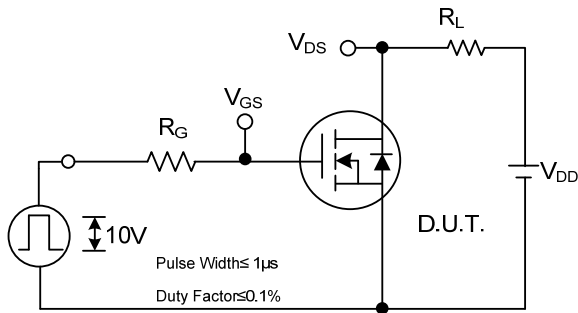
Peak Diode Recovery dv/dt Test Circuit



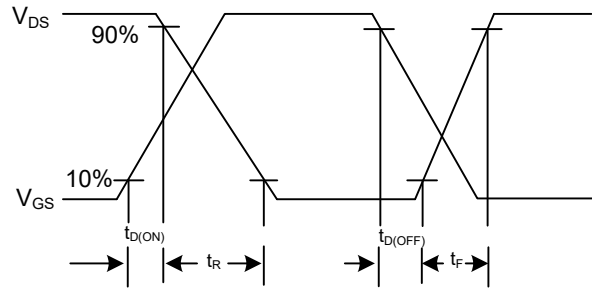
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

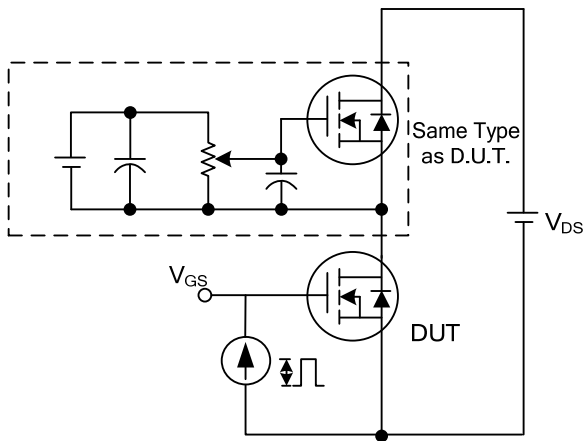
TEST CIRCUITS AND WAVEFORMS



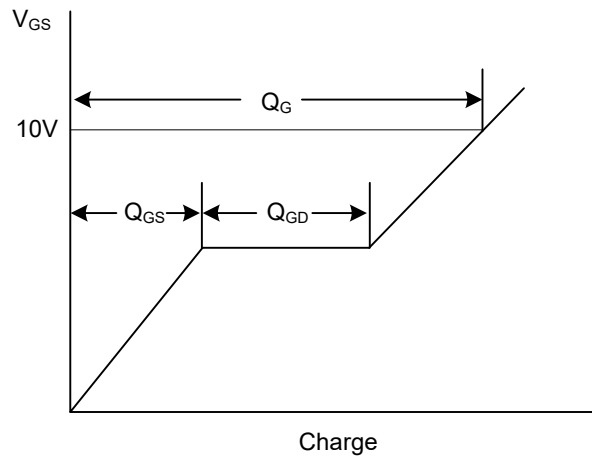
Switching Test Circuit



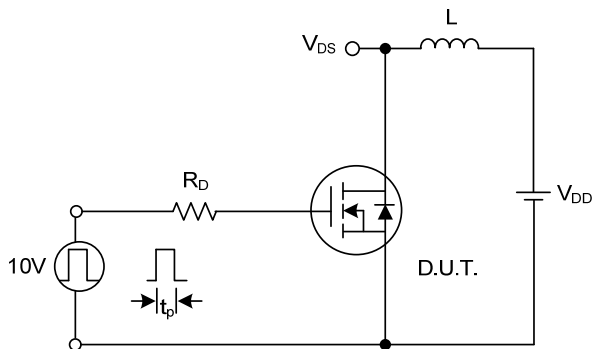
Switching Waveforms



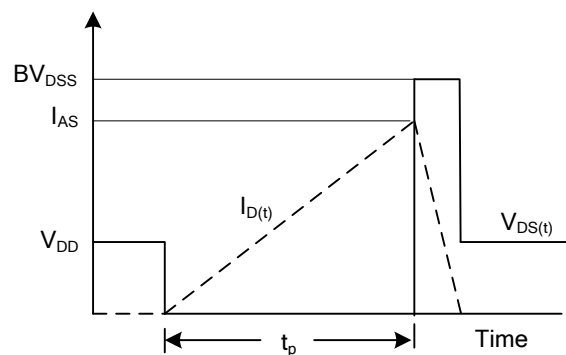
Gate Charge Test Circuit



Gate Charge Waveform

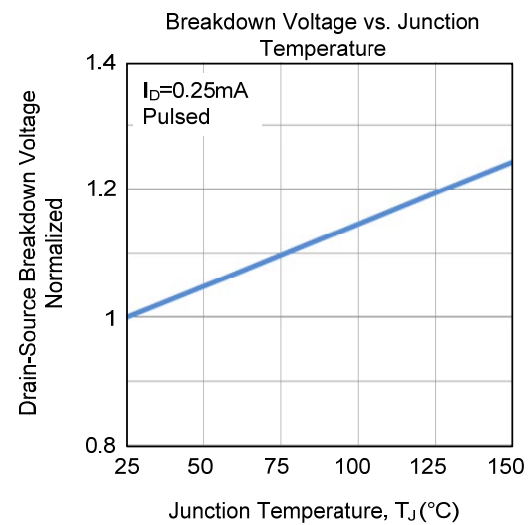
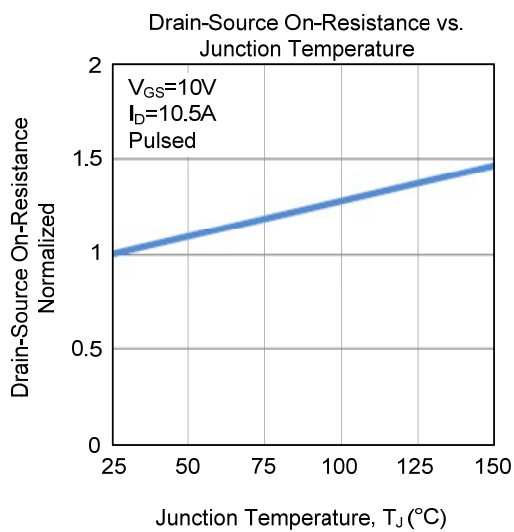
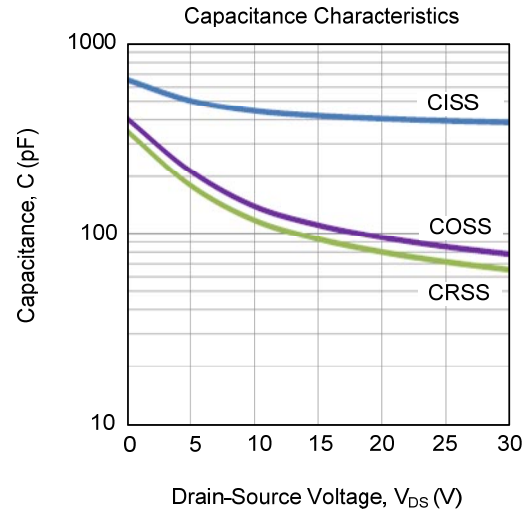
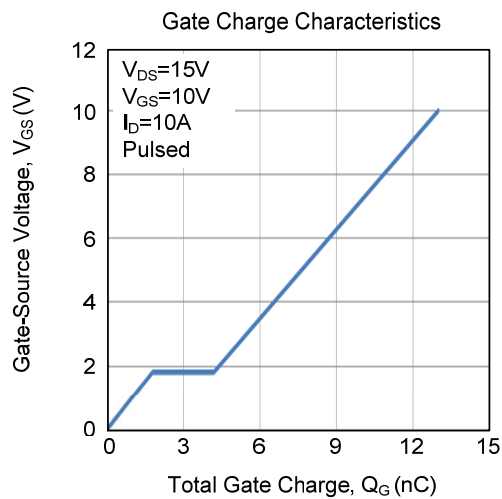
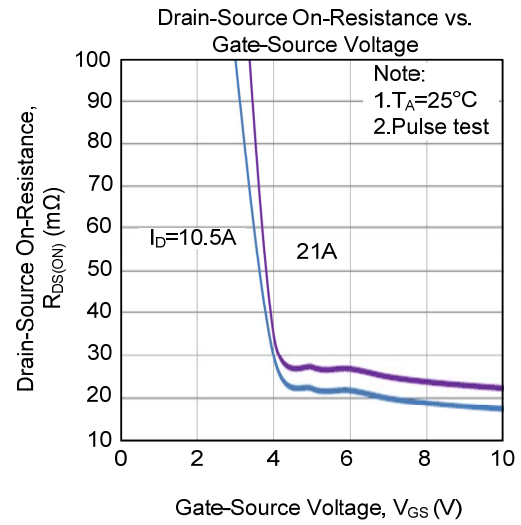
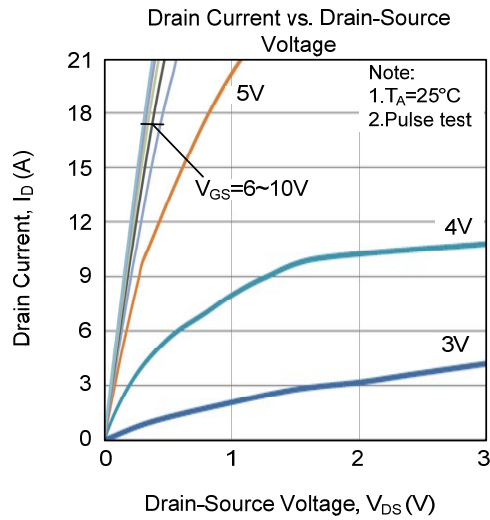


Unclamped Inductive Switching Test Circuit

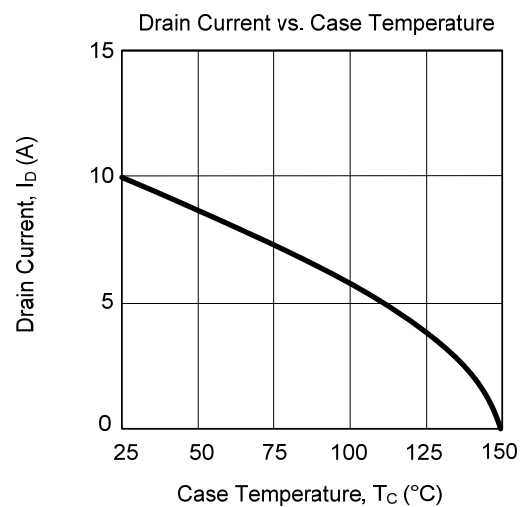
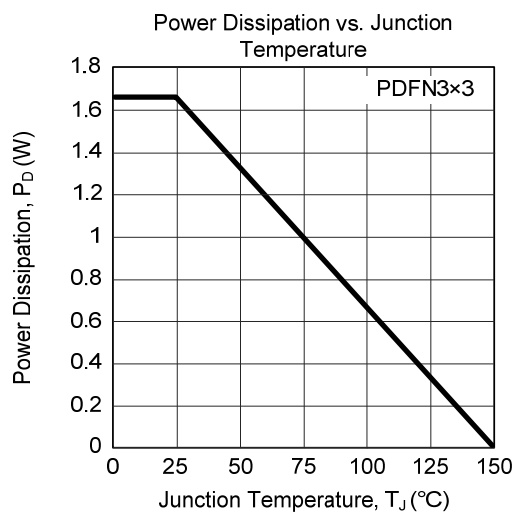
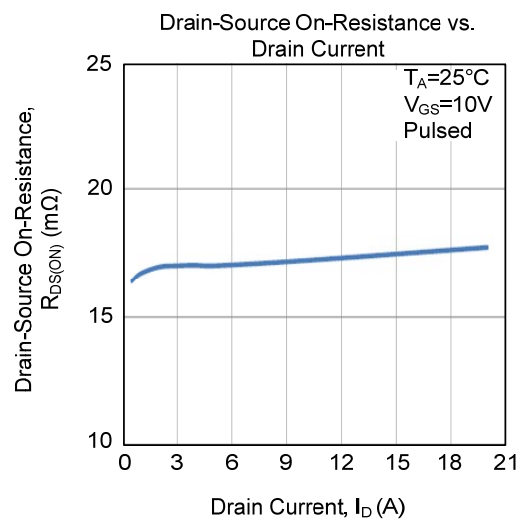
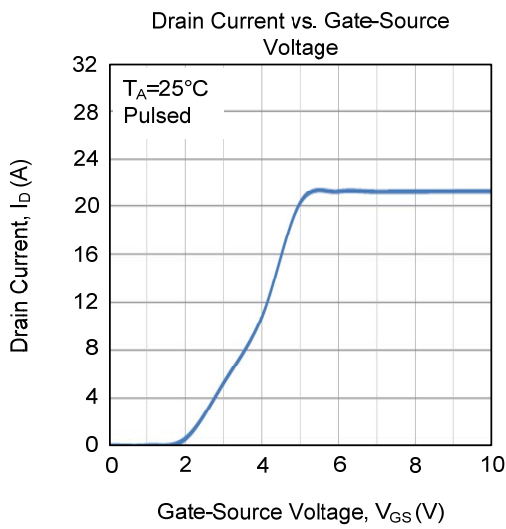
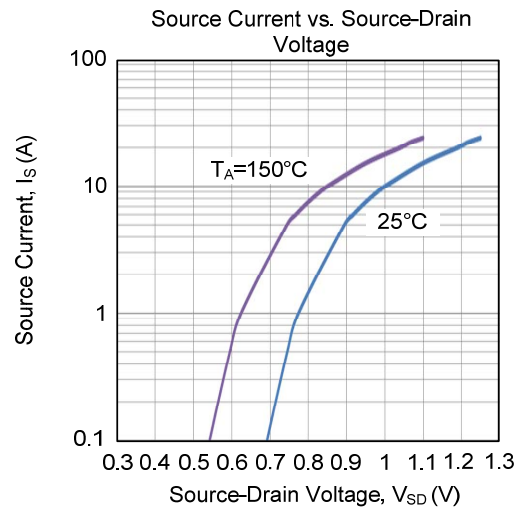
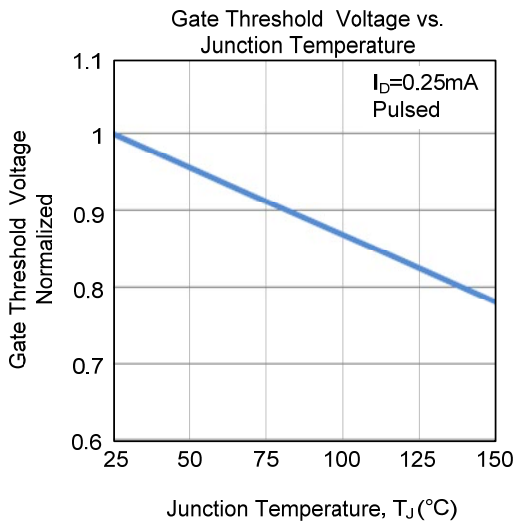


Unclamped Inductive Switching Waveforms

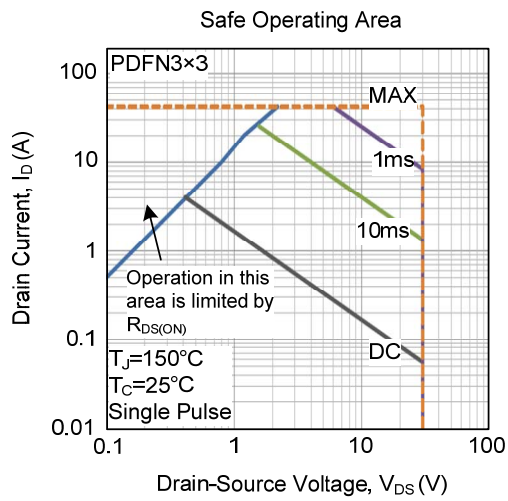
TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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