



UD05306

Preliminary

CMOS IC

2A, 2MHz, SYNCHRONOUS STEP-DOWN REGULATOR

DESCRIPTION

The UTC **UD05306** is CMOS-based, high efficiency synchronous, step-down DC/DC converter. Its input voltage range is from 2.8V to 5.5V and provides an adjustable regulated output voltage from 0.8V to 5V while delivering up to 2A of output current.

The internal synchronous rectifier with low R_{ON} power switches dramatically reduces conduction loss at PWM. Internal integrated power switches also increase efficiency and eliminate the need for an external Schottky diode. Switching frequency could be set by an external resistor or can be synchronized to an external clock. 100% duty cycle provides low dropout operation extending battery life in portable systems.

UTC **UD05306** operation in forced continuous PWM Mode which minimizes ripple voltage and reduces the noise and RF interference. 100% duty cycle in Low Dropout Operation further maximize battery life.

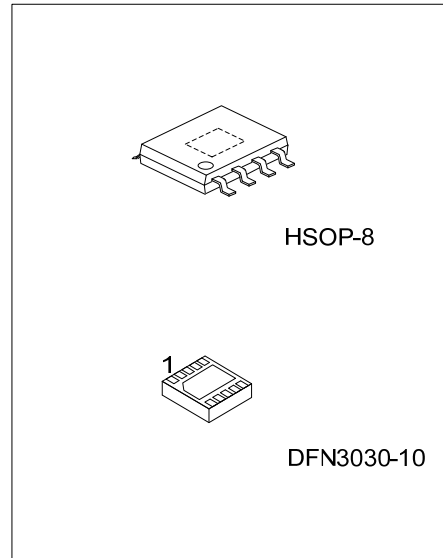
FEATURES

- * High Efficiency: Up to 95%
- * Low Dropout Operation: 100% Duty Cycle
- * Programmable Frequency: 300kHz~2MHz
- * No Schottky Diode Required
- * 0.8V Reference Allows Low Output Voltage
- * Low RDS (ON) Internal Switches: 110mW
- * Forced Continuous Mode Operation

ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UD05306L-SH2-R	UD05306G-SH2-R	HSOP-8	Tape Reel
UD05306L-K10-3030-R	UD05306G-K10-3030-R	DFN3030-10	Tape Reel

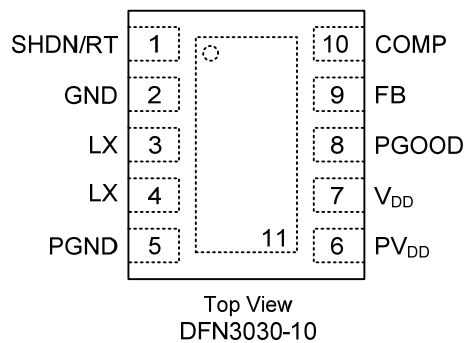
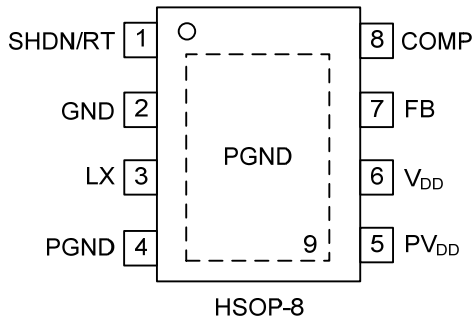
<p>UD05306G-SH2-R</p> <p>(1)Packing Type (2)Package Type (3)Green Package</p>	<p>(1) R: Tape Reel (2) SH2: HSOP-8, K10-3030: DFN3030-10 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING

HSOP-8	DFN3030-10
<p> UTC □□□□ → Date Code UD05306 □ → L: Lead Free □ → G: Halogen Free ● □□□□ → Lot Code </p>	<p> UD 05306 ● □□□□ → Date Code </p>

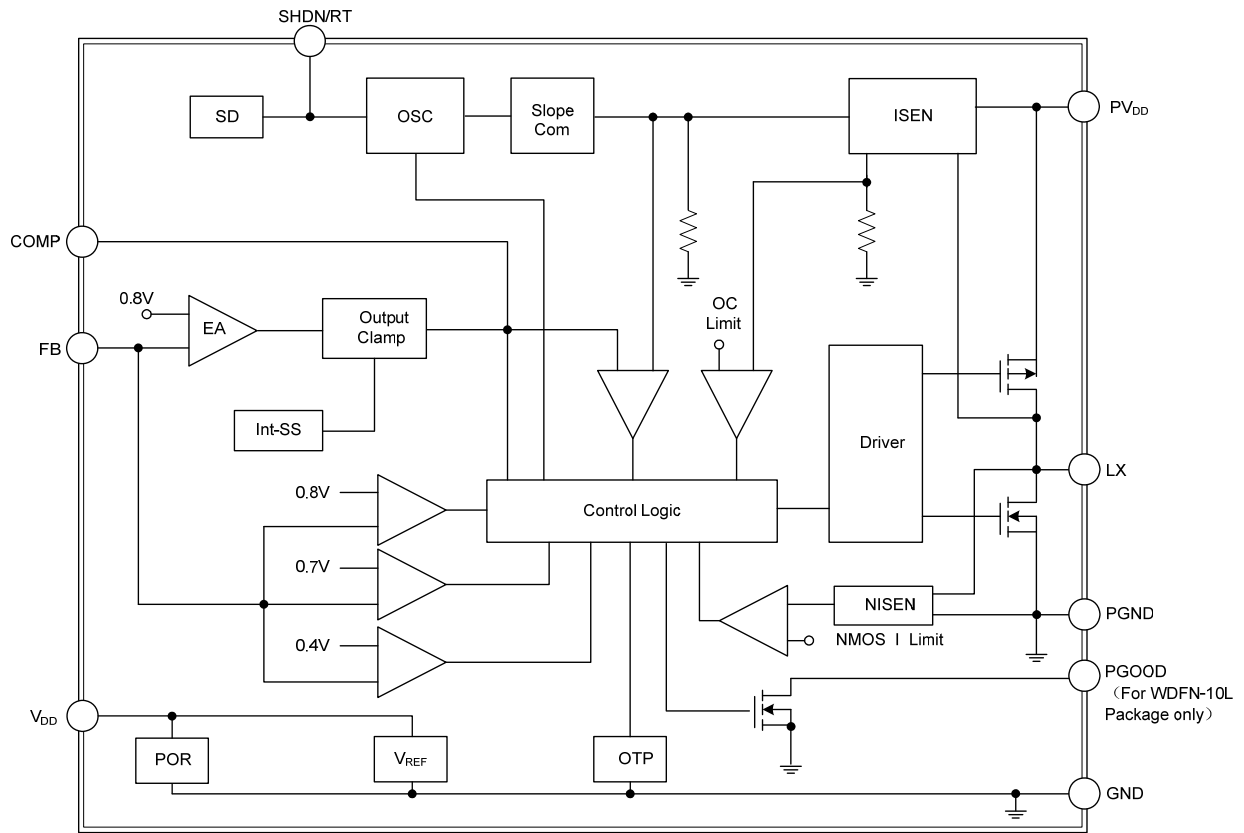
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.		PIN NAME	DESCRIPTION
HSOP-8	DFN3030-10		
1	1	SHDN/RT	Oscillator frequency sets with connecting a resistor from this PIN to ground. Forcing this PIN to V_{DD} causes the device to be shut down.
2	2	GND	Signal Ground. All small-signal components should connect to this ground, which in turn connects to PGND at one point.
3	3, 4	LX	Internal Power Switches Output. Connect this pin to the inductor.
4, 9	5	PGND	Power Ground. Connect this pin as closer as possible to the minus terminal of CIN and COUT.
5	6	PV_{DD}	Power Input Supply. Decouple this pin to PGND with a capacitor.
6	7	V_{DD}	Signal Input Supply. Decouple this pin to GND with a capacitor.
-	8	PGOOD	Power Good Indicator. This is an open-drain output pin, if V_{out} exceed $\pm 12.5\%$ of regulation point, this pin will pulled to ground.
7	9	FB	Feedback Pin. The V_{FB} voltage received from a resistive divider connected across the output.
8	10	COMP	Error Amplifier Compensation Point. Connect external compensation elements to this pin to stabilize the control loop.
-	11	NC	No Internal Connection. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Input Voltage, V_{DD} , PV_{DD}	V_{IN}	6	V
LX Pin Switch Voltage	V_{LX}	6	V
Other I/O Pin Voltages		6	V
LX Pin Switch Current	I_{LX}	4	A
Power Dissipation @ $T_A=25^\circ\text{C}$	P_D	1.33	W
Junction Temperature	T_J	+150	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	75	$^\circ\text{C/W}$
Junction to Case	θ_{JC}	15	$^\circ\text{C/W}$

■ RECOMMENDED OPERATING CONDITIONS (Note 4)

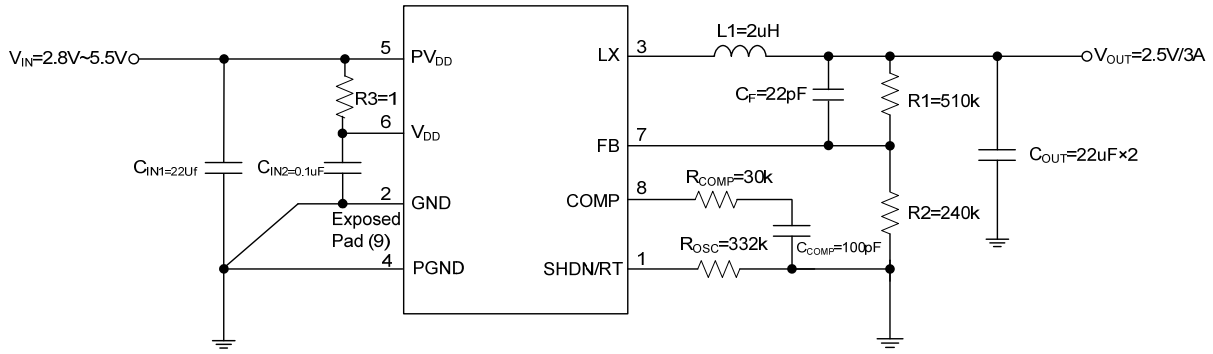
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Input Voltage	V_{IN}	2.8 ~ 5.5	V
Junction Temperature Range	T_J	-40 ~ +125	$^\circ\text{C}$
Ambient Temperature Range	T_A	-40 ~ +85	$^\circ\text{C}$

Note: The device is not guaranteed to function outside its operating conditions.

■ ELECTRICAL CHARACTERISTICS ($V_{DD}=3.3\text{V}$, $T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{DD}		2.8		5.5	V
Feedback Reference Voltage	V_{REF}		0.784	0.8	0.816	V
DC Bias Current	I_{DC}	Active, $V_{FB}=0.78\text{V}$, Not Switching		460		μA
	I_{SD}	Shutdown			1	μA
Output Voltage Line Regulation	ΔV_{LINE}	$V_{IN}=2.7\text{V}\sim 5.5\text{V}$		0.07		$\%/V$
Output Voltage Load Regulation	ΔV_{LOAD}	$0\text{A}<I_{LOAD}<3\text{A}$		0.5		%
Current Sense Transresistance	R_T			0.4		Ω
Power Good Range				± 12.5	± 15	%
Power Good Pull-Down Resistance	R_{PD}				120	Ω
Switching Frequency	F_{SW}	$R_{OSC}=332\text{k}$	0.8	1	1.2	MHz
		Switching Frequency	0.3		2	MHz
Switch On Resistance, High	R_{PMOS}	$I_{SW}=0.5\text{A}$		110	160	$\text{m}\Omega$
Switch On Resistance, Low	R_{NMOS}	$I_{SW}=0.5\text{A}$		110	170	$\text{m}\Omega$
Peak Current Limit	I_{LIM}		3.2	3.8		A
Under Voltage Lockout Threshold		V_{DD} Rising		2.4		V
		V_{DD} Falling		2.3		V
Shutdown Threshold	$V_{SHDN/RT}$			$V_{IN}-0.7$	$V_{IN}-0.4$	V

■ TYPICAL APPLICATION CIRCUIT



Note: Using all Ceramic Capacitors

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