



# UTT50N03L

**Power MOSFET**

## 50A, 30V N-CHANNEL POWER MOSFET

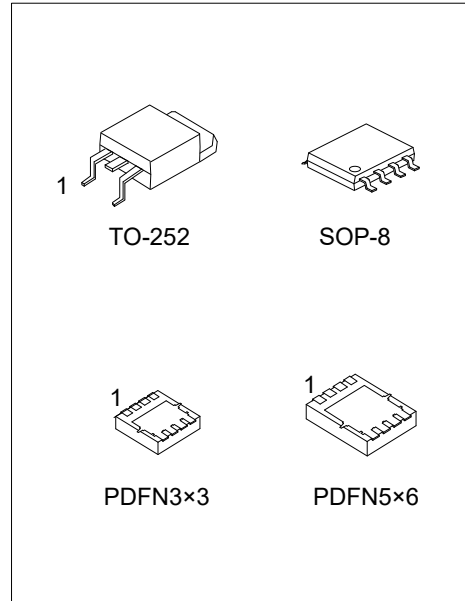
### DESCRIPTION

The UTC **UTT50N03L** is an N-channel power MOSFET using UTC's advanced technology to provide customers with a minimum on-state resistance and superior switching performance.

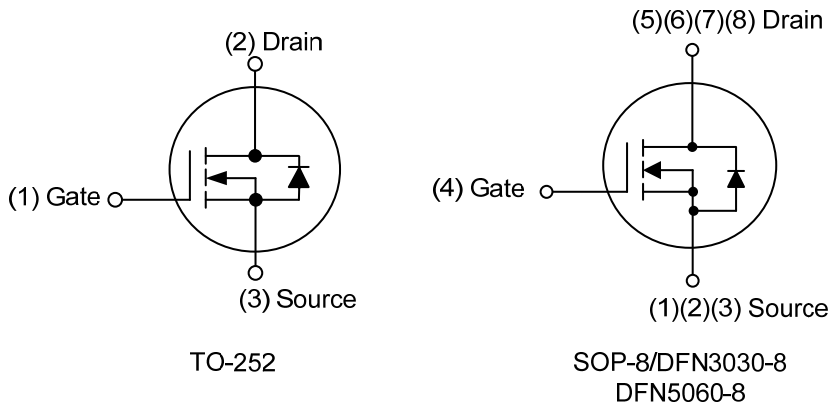
The UTC **UTT50N03L** is generally applied in low power switching mode power appliances and electronic ballast.

### FEATURES

- \*  $R_{DS(ON)} \leq 7.8 \text{ m}\Omega @ V_{GS}=10V, I_D=12A$
- $R_{DS(ON)} \leq 13 \text{ m}\Omega @ V_{GS}=4.5V, I_D=9.0A$
- \* High Switching Speed
- \* Improved dv/dt capability



### SYMBOL



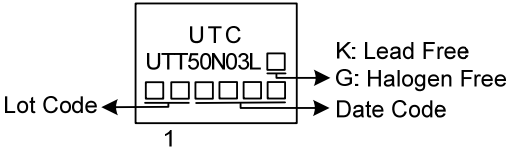
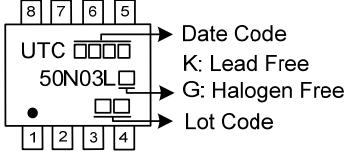
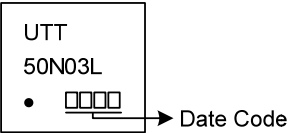
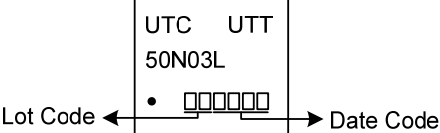
### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UTT50N03LK-TN3-R	UTT50N03LG-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
UTT50N03LK-S08-R	UTT50N03LG-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel
UTT50N03LK-P3030-R	UTT50N03LG-P3030-R	PDFN3×3	S	S	S	G	D	D	D	D	Tape Reel
UTT50N03LK-P5060-R	UTT50N03LG-P5060-R	PDFN5×6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UTT50N03LG-TN3-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) TN3: TO-252, S08: SOP-8, P3030: PDFN3×3 P5060: PDFN5×6</p> <p>(3) G: Halogen Free and Lead Free, K: Lead Free</p>
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■ MARKING

TO-252	SOP-8
 <p>Diagram showing marking on a TO-252 package. The marking includes 'UTC', 'UTT50N03L', a lead-free symbol (K), a halogen-free symbol (G), and a date code. A lot code is indicated by five squares on the left, and a date code is indicated by three squares on the right. A '1' is shown below the package.</p>	 <p>Diagram showing marking on an SOP-8 package. The marking includes 'UTC', '50N03L', a lead-free symbol (K), a halogen-free symbol (G), and a date code. A lot code is indicated by two squares on the right. The date code is indicated by three squares at the top, and the lot code is indicated by two squares at the bottom.</p>
PDFN3x3	PDFN5x6
 <p>Diagram showing marking on a PDFN3x3 package. The marking includes 'UTT', '50N03L', and a date code indicated by three squares.</p>	 <p>Diagram showing marking on a PDFN5x6 package. The marking includes 'UTC UTT', '50N03L', a lot code indicated by five squares on the left, and a date code indicated by three squares on the right.</p>

■ ABSOLUTE MAXIMUM RATINGS ( $T_A=25^\circ\text{C}$ , unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{DSS}$	30	V
Gate-Source Voltage		$V_{GSS}$	$\pm 20$	V
Continuous Drain Current		$I_D$	50	A
Pulsed Drain Current (Note 2)		$I_{DM}$	100	A
Avalanche Energy	Single Pulsed (Note 3)	$E_{AS}$	7.2	mJ
Peak Diode Recovery dv/dt		dv/dt	10	V/ns
Power Dissipation	TO-252	$P_D$	2.5	W
	SOP-8		1.38	W
	PDFN3×3		1.66	W
	PDFN5×6		1.92	W
Junction Temperature		$T_J$	+150	$^\circ\text{C}$
Operation and Storage Temperature		$T_{STG}$	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3.  $L=0.1\text{mH}$ ,  $I_{AS}=12\text{A}$ ,  $V_{DD}=25\text{V}$ ,  $R_G=20\Omega$ , Starting  $T_J=25^\circ\text{C}$ .

4.  $I_{SD} \leq 30\text{A}$ ,  $V_{DS}=0\text{V}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$ .

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-252	$\theta_{JA}$	50	$^\circ\text{C}/\text{W}$
	SOP-8		125	$^\circ\text{C}/\text{W}$
	PDFN3×3		75	$^\circ\text{C}/\text{W}$
	PDFN5×6		65	$^\circ\text{C}/\text{W}$

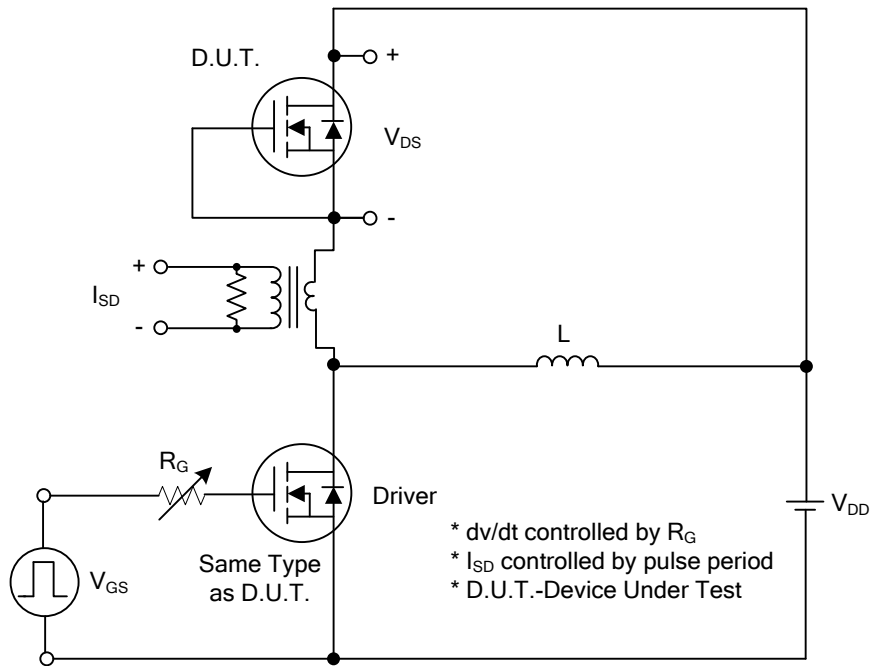
Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

■ ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C, unless otherwise specified)

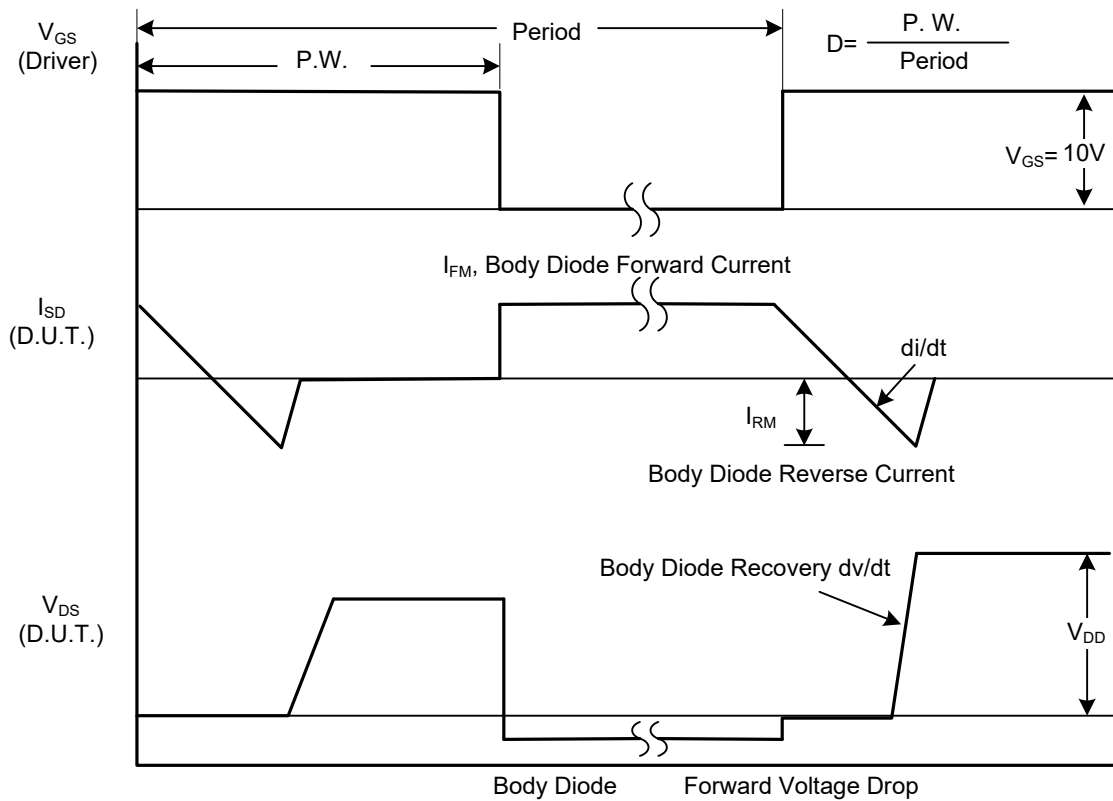
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	30			V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V			1	μA
Gate-Source Leakage Current	Forward	I <sub>GSS</sub> V <sub>GS</sub> =20V, V <sub>DS</sub> =0V			100	nA
	Reverse				-100	nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0		3.0	V
Static Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =12A		5.8	7.8	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =9.0A		9.0	13	mΩ
<b>DYNAMIC CHARACTERISTICS</b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		1280		pF
Output Capacitance	C <sub>OSS</sub>			270		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			229		pF
<b>SWITCHING CHARACTERISTICS</b>						
Total Gate Charge	Q <sub>G</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =10V, I <sub>D</sub> =50A I <sub>G</sub> =1mA (Note1,2)		44		nC
Gate-Source Charge	Q <sub>GS</sub>			5		nC
Gate-Drain Charge	Q <sub>GD</sub>			10.5		nC
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =10V, I <sub>D</sub> =50A, R <sub>G</sub> =3.3Ω (Note1,2)		7		ns
Turn-On Rise Time	t <sub>R</sub>			17		ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			33		ns
Turn-Off Fall Time	t <sub>F</sub>			23		ns
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
Maximum Continuous Drain-Source Diode Forward Current	I <sub>S</sub>				50	A
Maximum Pulsed Drain-Source Diode Forward Current	I <sub>SM</sub>				100	A
Drain-Source Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =50A, V <sub>GS</sub> =0V			1.5	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>S</sub> =30A, V <sub>GS</sub> =0V,		250		ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	dI <sub>S</sub> /dt=100A/μs		1200		nC

Notes: 1. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.  
 2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



Peak Diode Recovery dv/dt Test Circuit



Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS

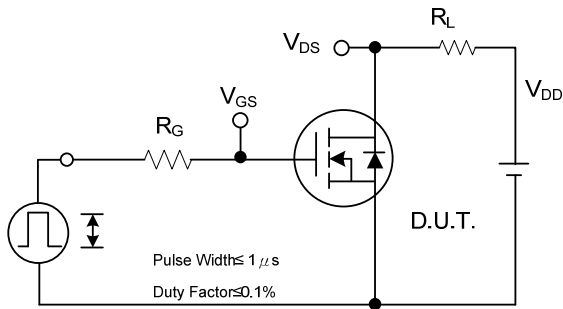


Fig. 2A Switching Test Circuit

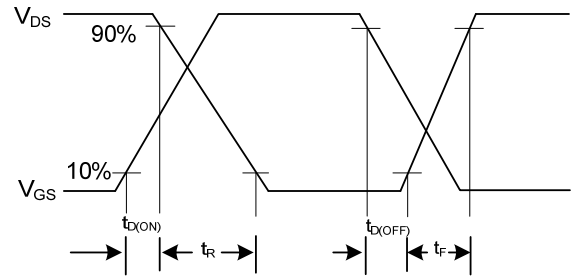


Fig. 2B Switching Waveforms

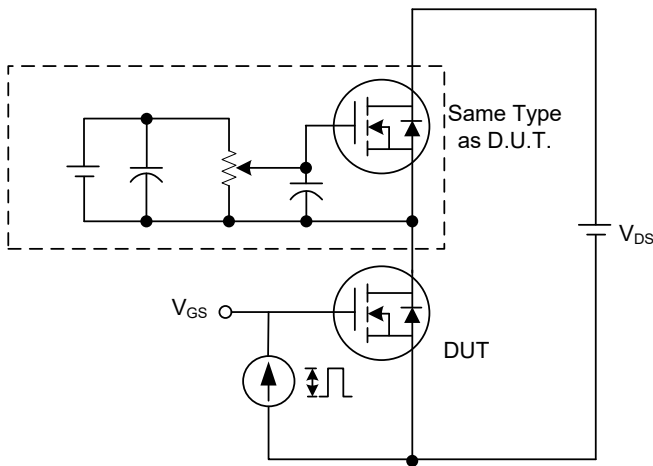


Fig. 3A Gate Charge Test Circuit

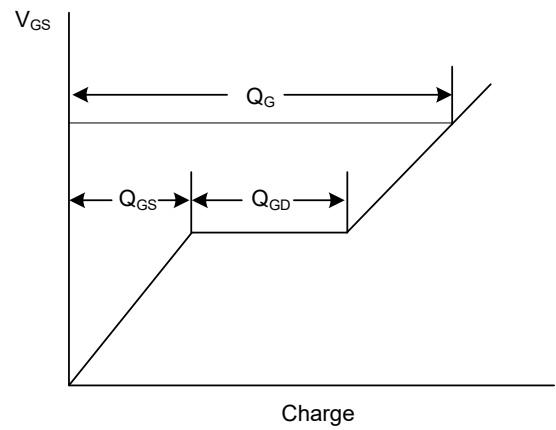


Fig. 3B Gate Charge Waveform

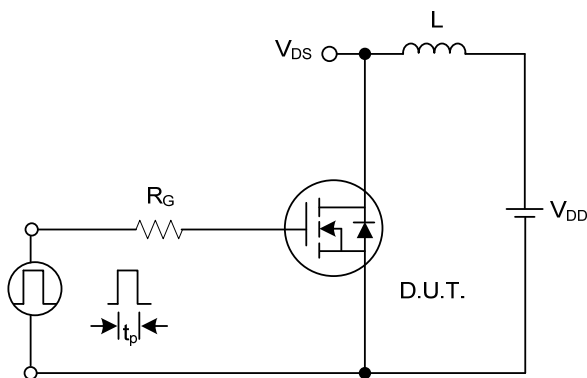


Fig. 4A Unclamped Inductive Switching Test Circuit

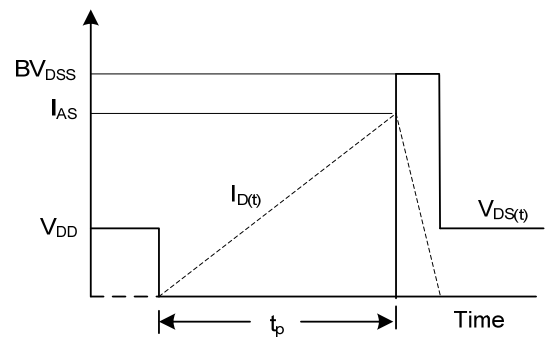
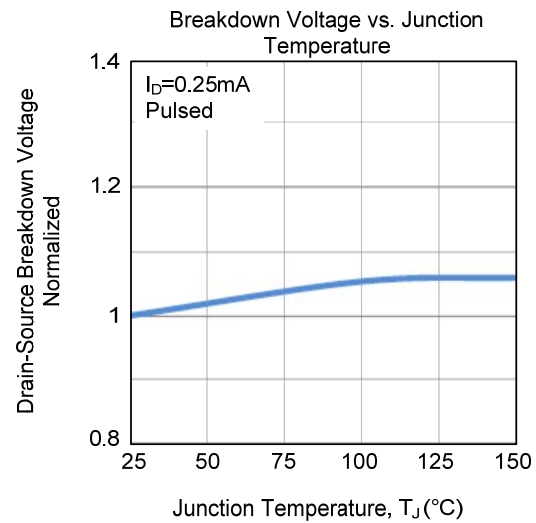
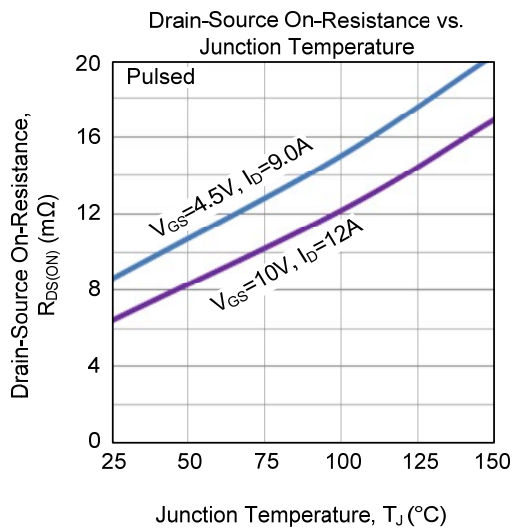
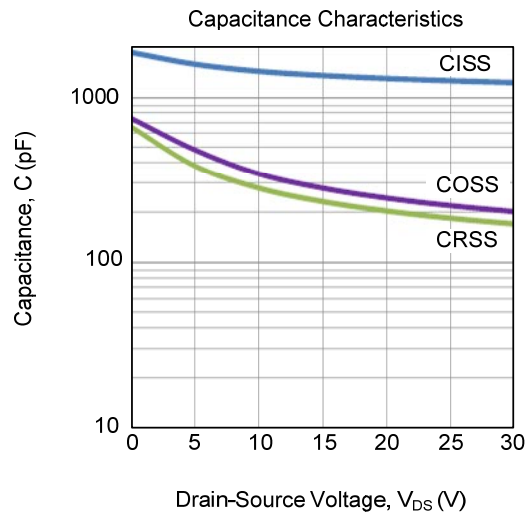
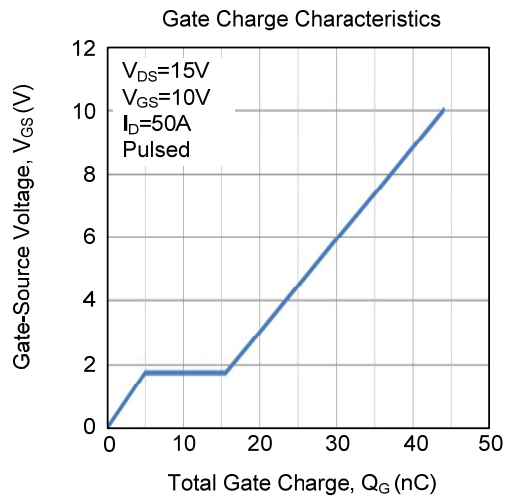
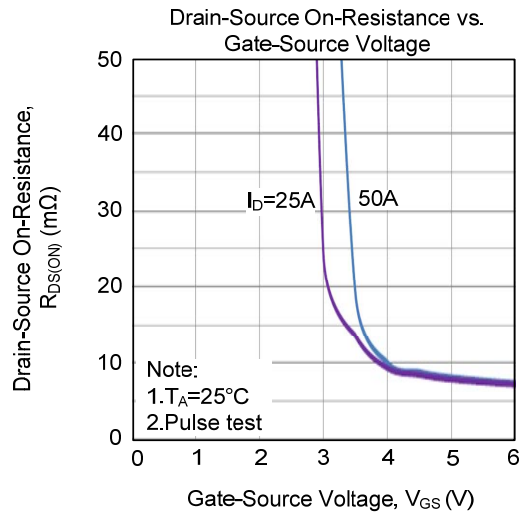
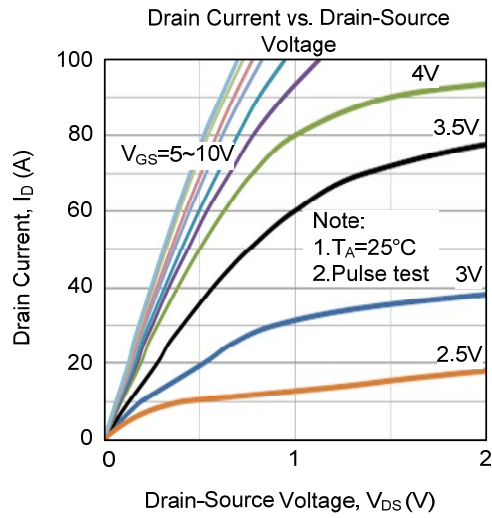
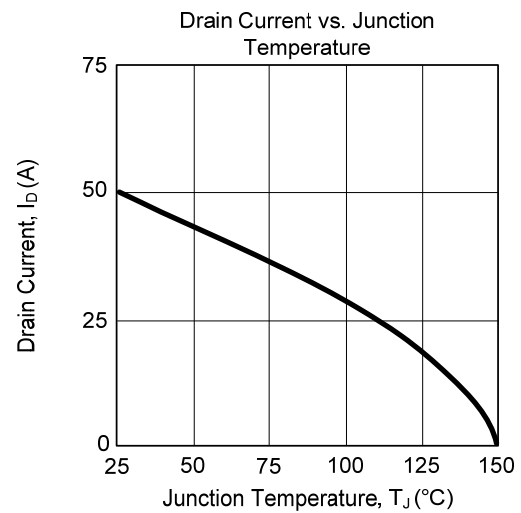
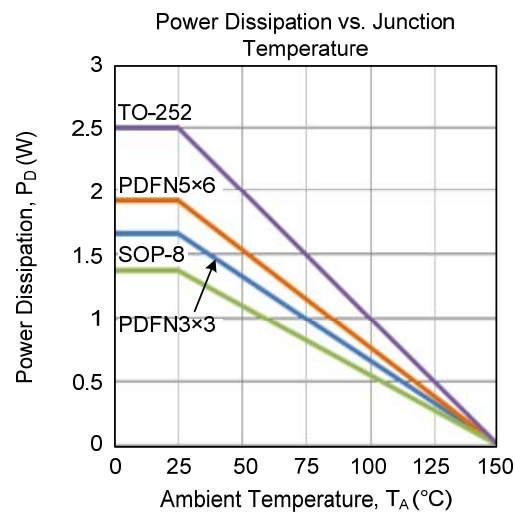
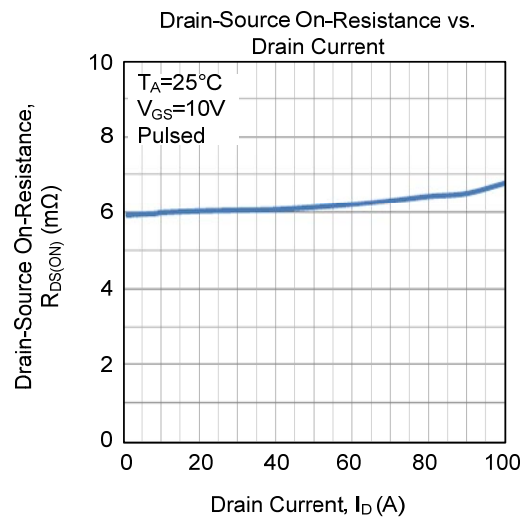
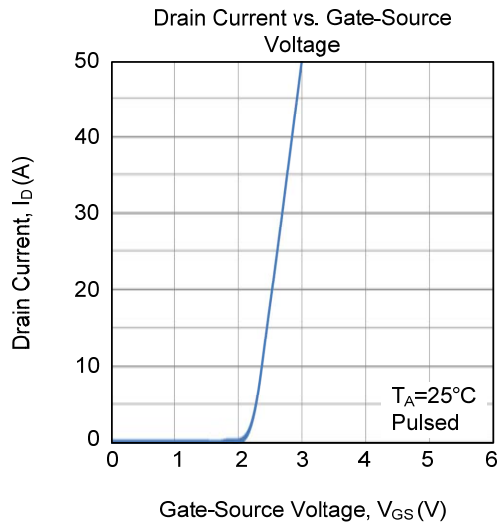
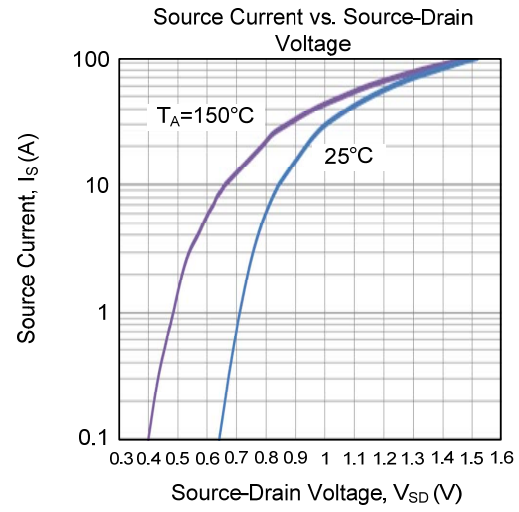
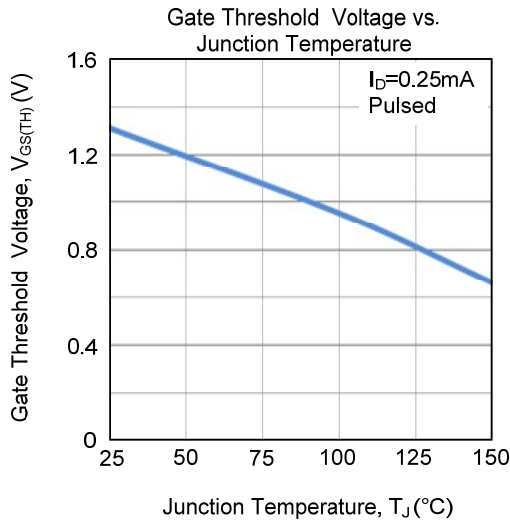


Fig. 4B Unclamped Inductive Switching Waveforms

## TYPICAL CHARACTERISTICS

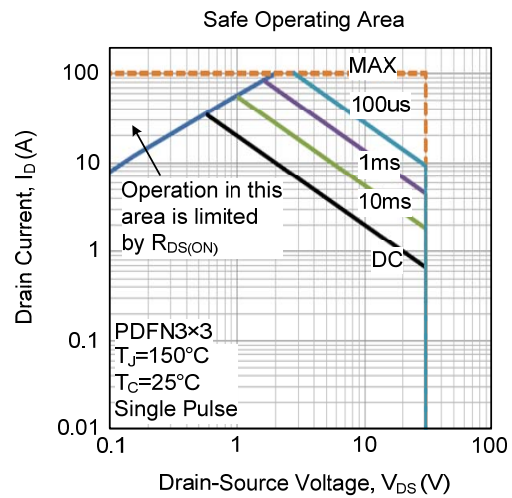
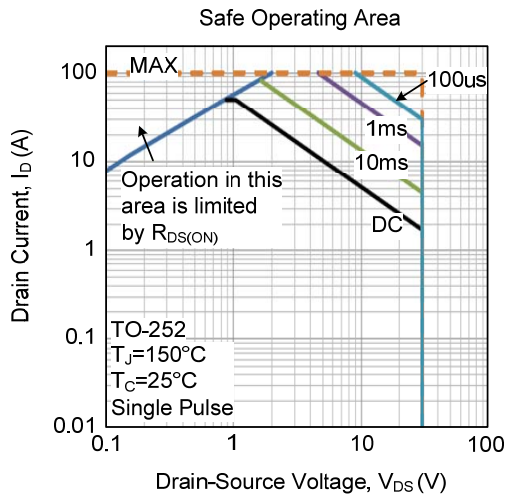


## TYPICAL CHARACTERISTICS (Cont.)





■ TYPICAL CHARACTERISTICS (Cont.)



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