



UD8N04Z

POWER MOSFET

5.2A, 40V N-CHANNEL ENHANCEMENT MODE TRENCH POWER MOSFET

■ DESCRIPTION

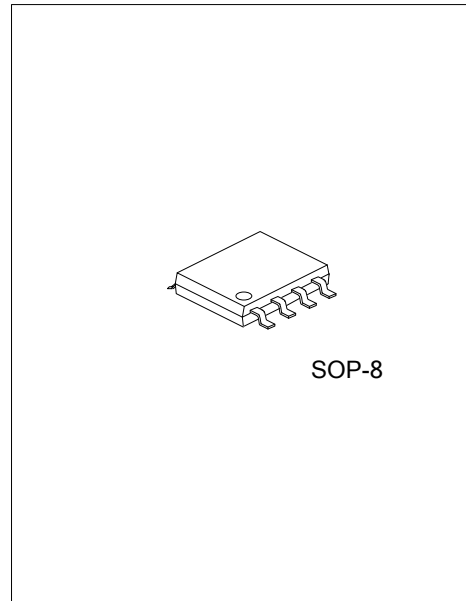
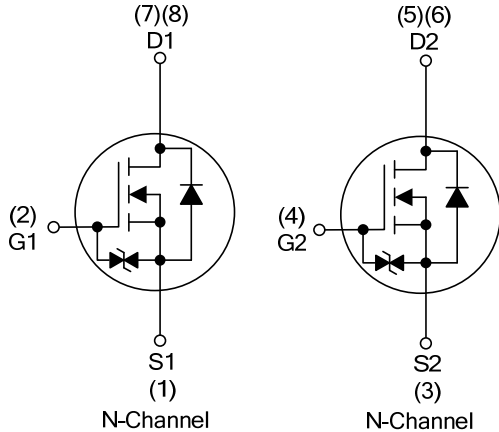
The UTC **UD8N04Z** is a N-channel enhancement mode power MOSFET using UTC's advanced technology to provide customers with an extremely low on-state resistance and superior switching performance.

The UTC **UD8N04Z** is suitable for high frequency DC-DC converters with synchronous rectification applications.

■ FEATURES

- * $R_{DS(ON)} \leq 85 \text{ m}\Omega @ V_{GS}=10\text{V}, I_D=5.2\text{A}$
- $R_{DS(ON)} \leq 112 \text{ m}\Omega @ V_{GS}=4.5\text{V}, I_D=4.0\text{A}$
- * High Power and Current Handling Capability
- * High Cell Density Trench Technology

■ SYMBOL



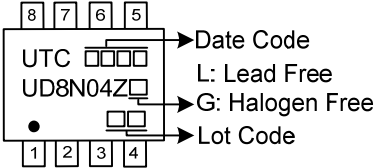
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment						Packing		
Lead Free	Halogen Free		1	2	3	4	5	6		7	8
UD8N04ZL-S08-R	UD8N04ZG-S08-R	SOP-8	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UD8N04ZG-S08-R</p> <ul style="list-style-type: none"> (1) Packing Type (2) Package Type (3) Green Package 	<ul style="list-style-type: none"> (1) R: Tape Reel (2) S08: SOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	40	V
Gate-Source Voltage		V_{GSS}	± 12	V
Continuous Drain Current	Continuous	I_D	5.2	A
Pulsed Drain Current (Note 2)	Pulsed	I_{DM}	8	A
Power Dissipation (Note 3)		P_D	1.47	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. Mounted on a ceramic board.

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	85	$^\circ\text{C/W}$

Note: Mounted on a ceramic board.

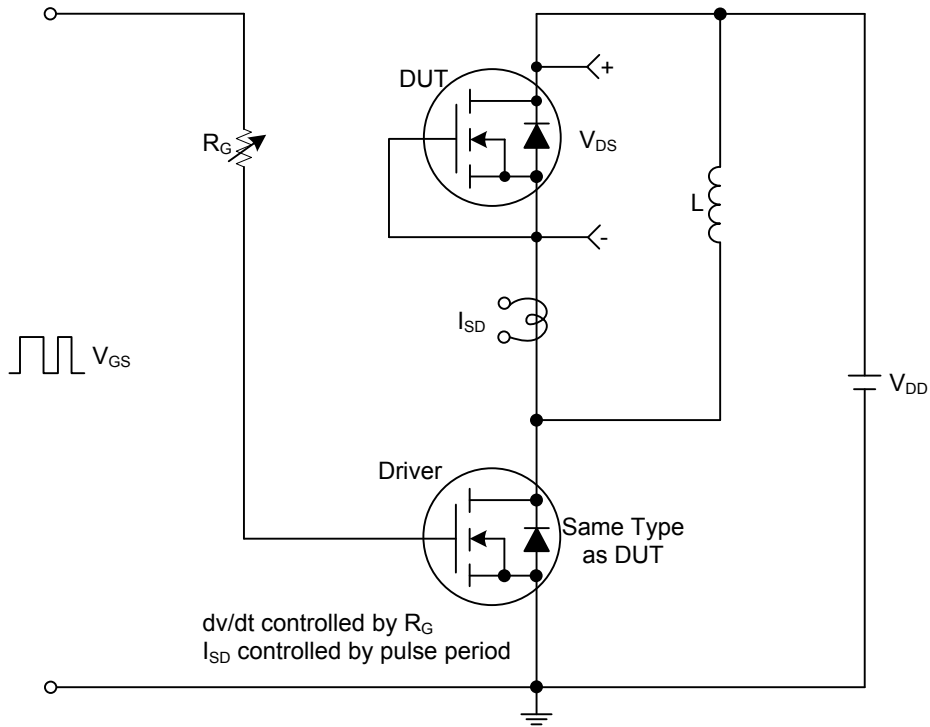
■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	40			V
Drain-Source Leakage Current		I_{DSS}	$V_{DS}=40\text{V}$, $V_{GS}=0\text{V}$			1	μA
Gate-Source Leakage Current	Forward	I_{GSS}	$V_{GS}=+12\text{V}$, $V_{DS}=0\text{V}$			+10	μA
	Reverse		$V_{GS}=-12\text{V}$, $V_{DS}=0\text{V}$			-10	μA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=1\text{mA}$	1.0		3.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=5.2\text{A}$			85	$\text{m}\Omega$
			$V_{GS}=4.5\text{V}$, $I_D=4.0\text{A}$			112	$\text{m}\Omega$
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=10\text{V}$, $f=1.0\text{MHz}$		370		pF
Output Capacitance		C_{OSS}			69		pF
Reverse Transfer Capacitance		C_{RSS}			48		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q_G	$V_{DS}=20\text{V}$, $V_{GS}=5.0\text{V}$, $I_D=4.0\text{A}$, $I_G=1\text{mA}$ (Note 1, 2)		5.3		nC
Gate to Source Charge		Q_{GS}			2.1		nC
Gate to Drain Charge		Q_{GD}			0.8		nC
Turn-on Delay Time (Note 1)		$t_{D(ON)}$	$V_{DD}=20\text{V}$, $V_{GS}=10\text{V}$, $I_D=2.0\text{A}$, $R_G=10\Omega$ (Note 1, 2)		6.6		ns
Rise Time		t_R			14		ns
Turn-off Delay Time		$t_{D(OFF)}$			33		ns
Fall-Time		t_F			24		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				1.6	A
Maximum Body-Diode Pulsed Current		I_{SM}				8	A
Drain-Source Diode Forward Voltage (Note 1)		V_{SD}	$I_S=4.0\text{A}$, $V_{GS}=0\text{V}$			1.2	V

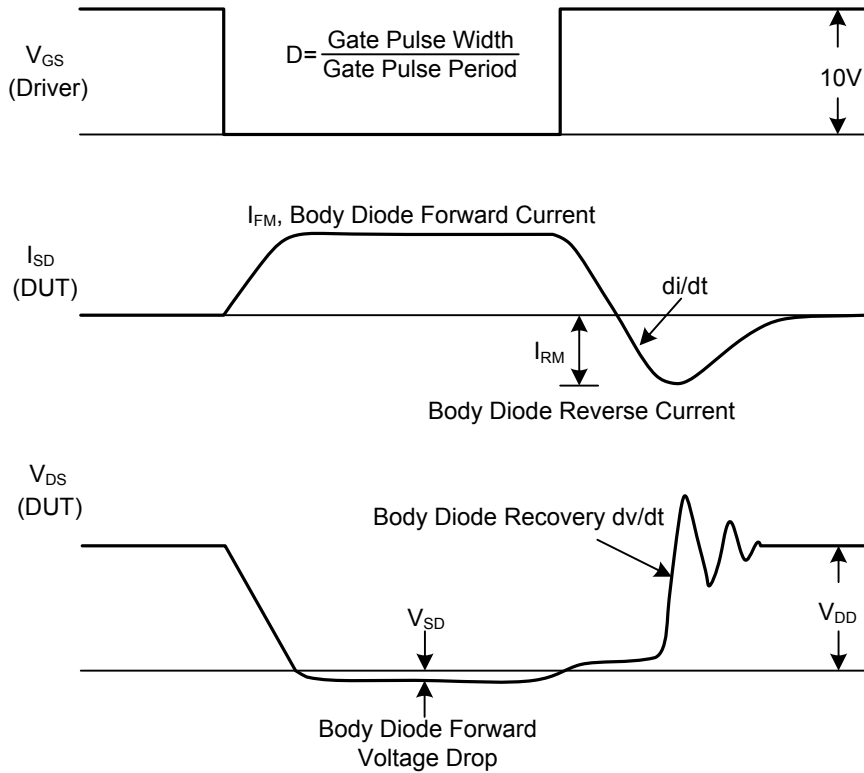
Notes: 1. Pulse Test: Pulse width $\leq 10\mu\text{s}$, Duty cycle $\leq 1\%$.

2. Essentially independent of operating temperature.

TEST CIRCUITS AND WAVEFORMS



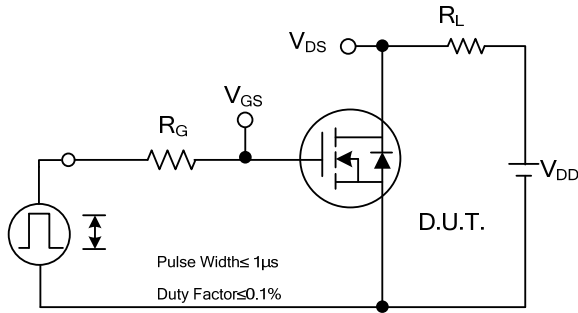
Peak Diode Recovery dv/dt Test Circuit



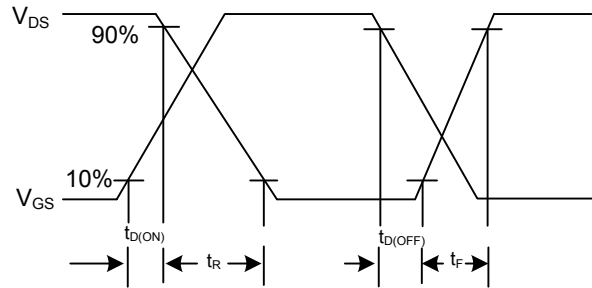
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

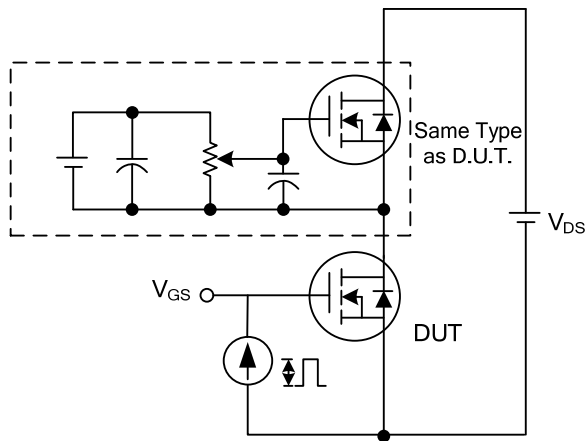
TEST CIRCUITS AND WAVEFORMS



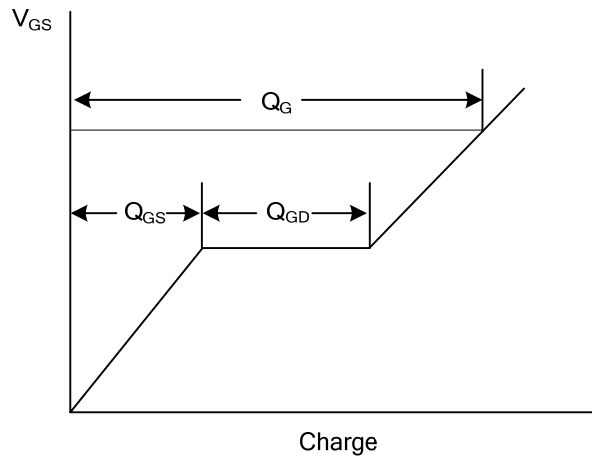
Switching Test Circuit



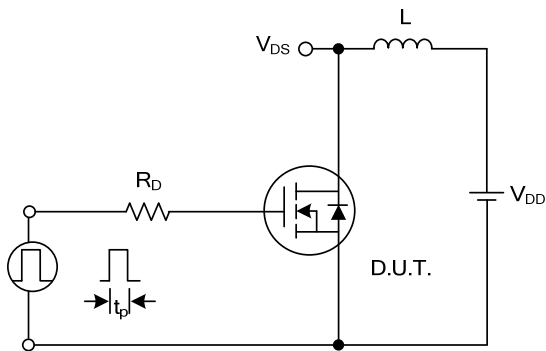
Switching Waveforms



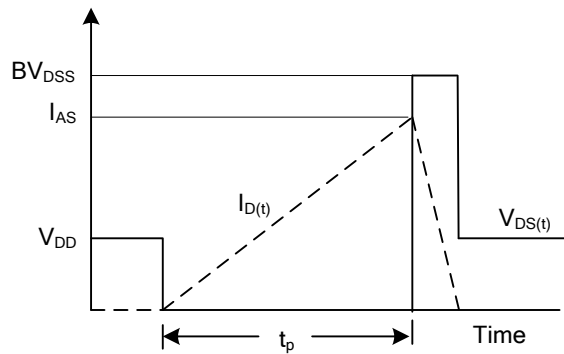
Gate Charge Test Circuit



Gate Charge Waveform

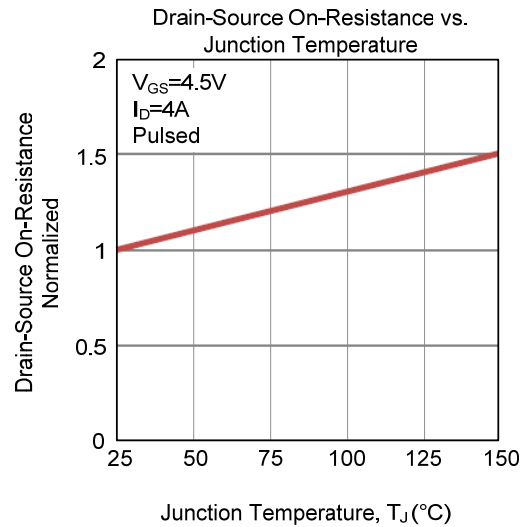
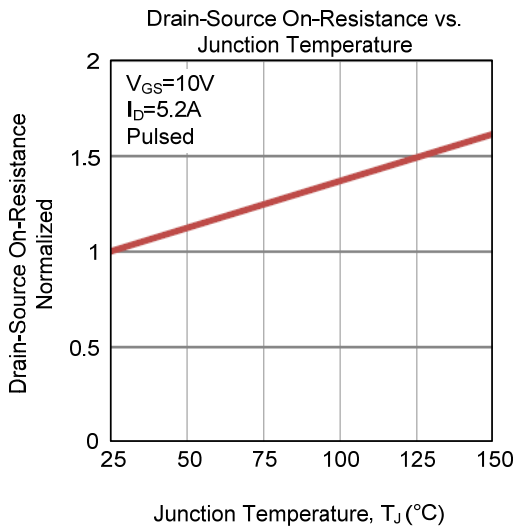
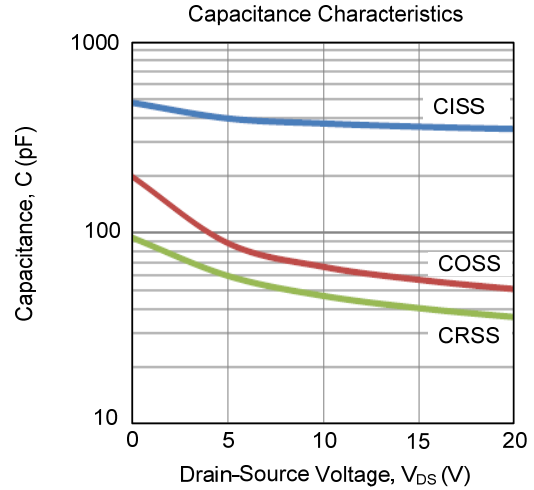
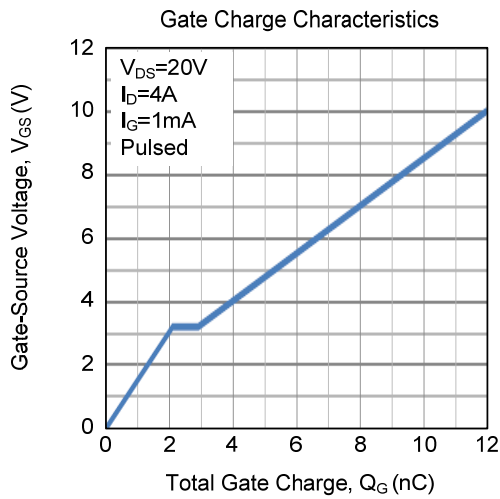
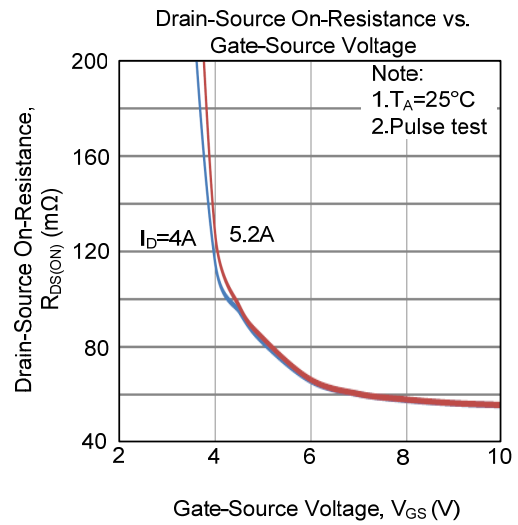
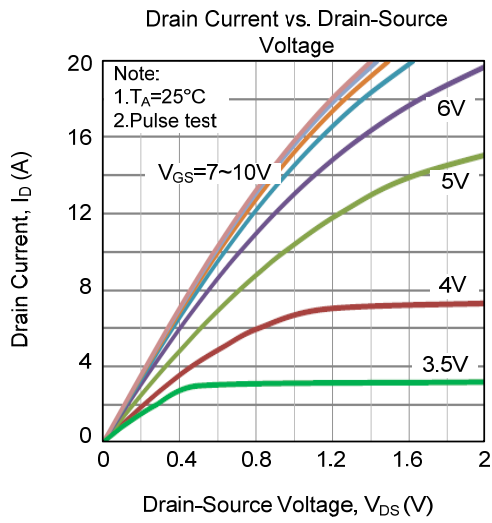


Unclamped Inductive Switching Test Circuit

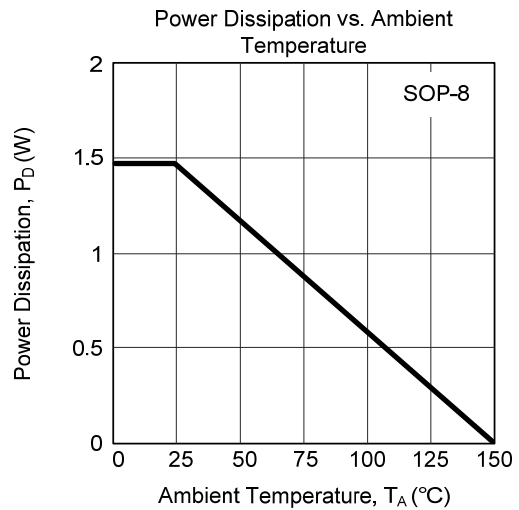
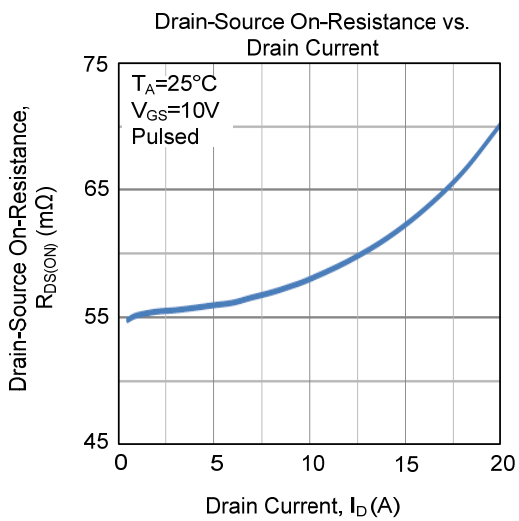
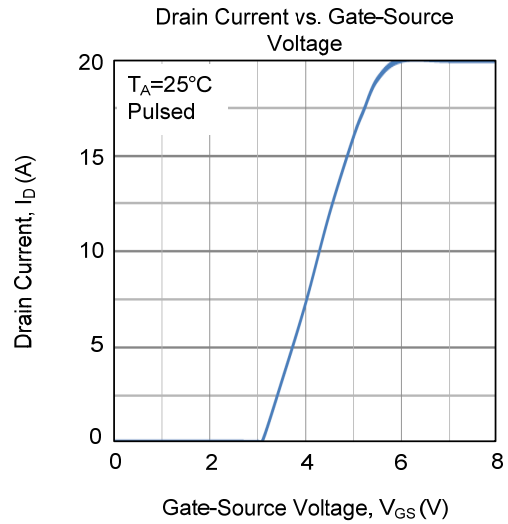
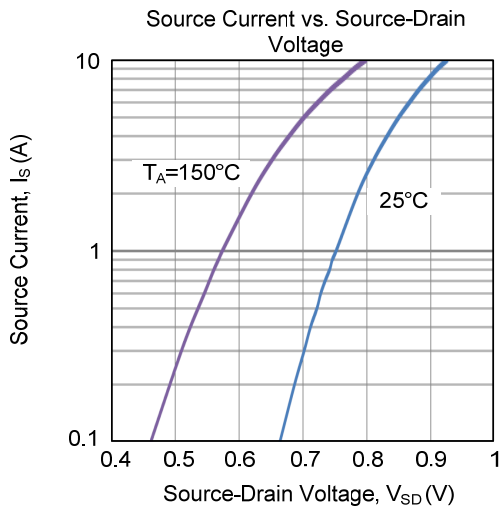
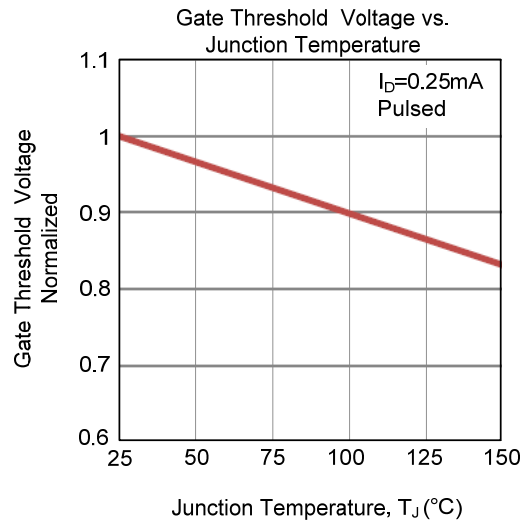
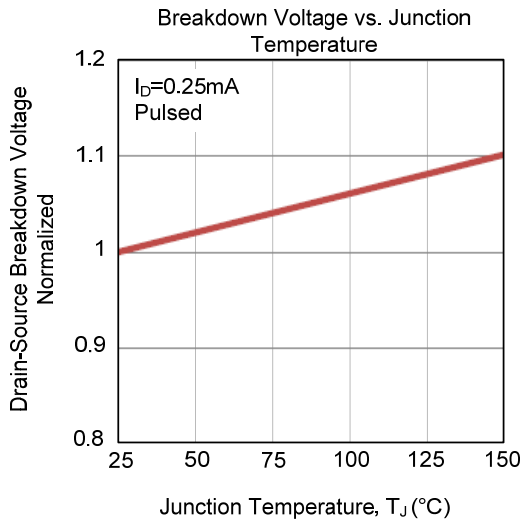


Unclamped Inductive Switching Waveforms

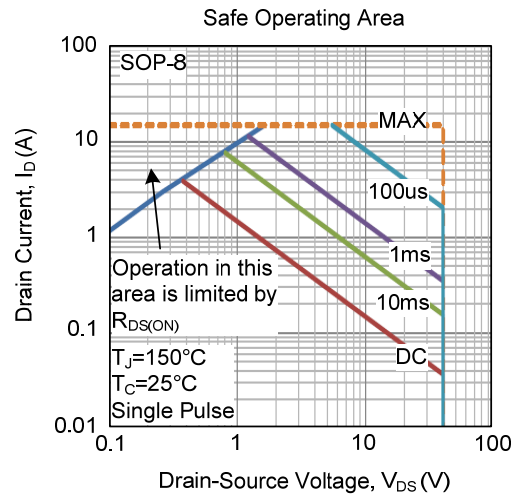
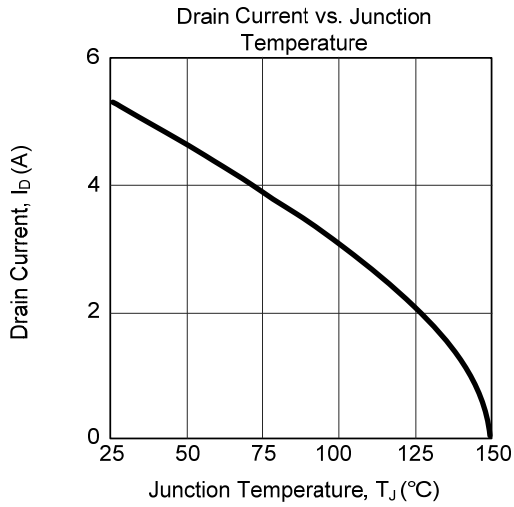
TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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