



UF3055-Q

Power MOSFET

3.0A, 60V N-CHANNEL ENHANCEMENT MODE POWER MOSFET

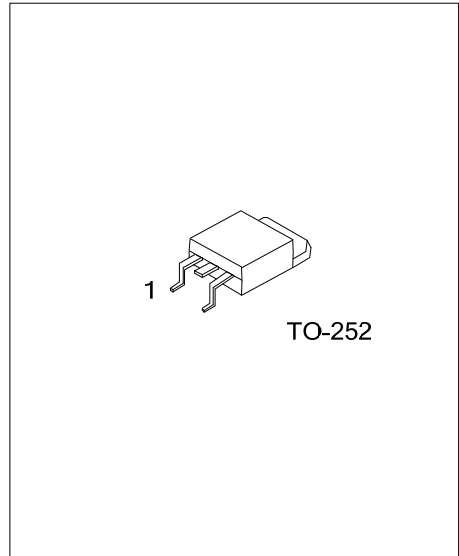
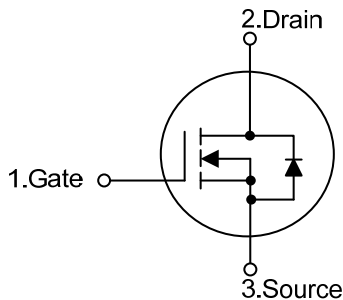
■ DESCRIPTION

As an N-channel enhancement mode power MOSFET, the UTC **UF3055-Q** is designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

■ FEATURES

* $R_{DS(ON)} < 0.14 \Omega @ V_{GS} = 10V, I_D = 1.5A$

■ SYMBOL



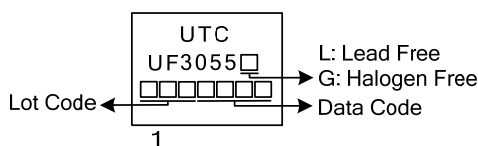
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UF3055L-TN3-R	UF3055G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UF3055G-TN3-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) TN3: TO-252</p> <p>(3) G: Halogen Free and Lead Free L: Lead Free</p>
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■ MARKING



■ ABSOLUTE MAXIMUM RATING ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	60	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous	I_D	3	A
	Pulsed (Note 2)	I_{DM}	9	A
Avalanche Energy (Note 3)	Single Pulsed (Note 3)	E_{AS}	45	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	15.4	V/ns
Power Dissipation		P_D	20	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 3.0 \text{ mH}$, $I_{AS} = 5.5 \text{ A}$, $V_{DD} = 50 \text{ V}$, $R_G = 25 \Omega$, Starting $T_J = 25^{\circ}\text{C}$.

4. $I_{SD} \leq 3.0 \text{ A}$, $di/dt \leq 200 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J = 25^{\circ}\text{C}$.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	110	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	6.3	$^{\circ}\text{C}/\text{W}$

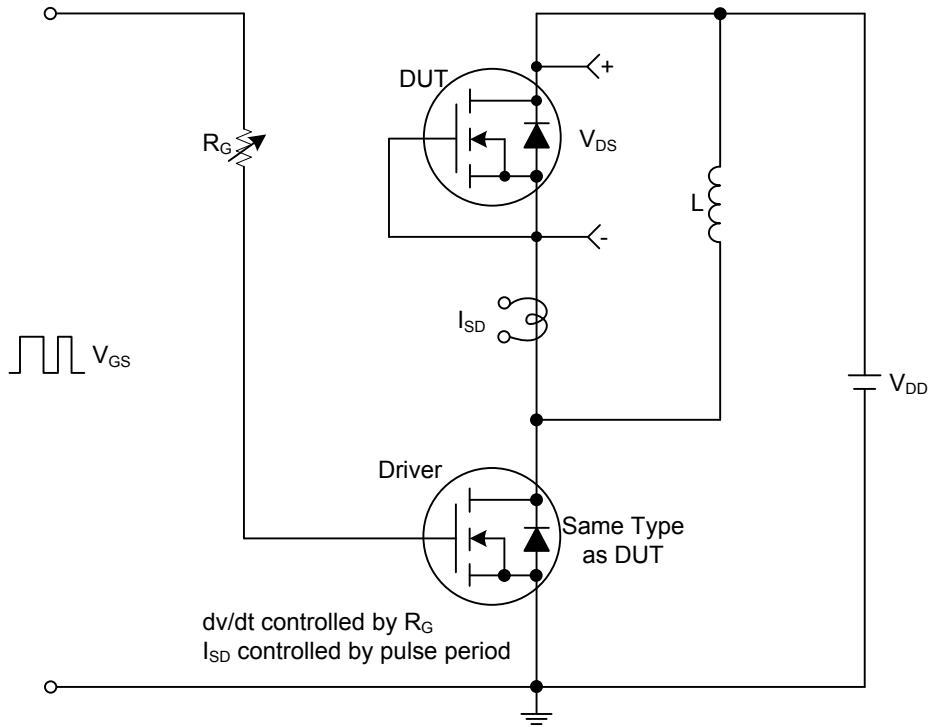
■ ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$	60			V
Drain-Source Leakage Current	I_{DSS}	$V_{GS} = 0\text{V}$, $V_{DS} = 60\text{V}$			1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0\text{V}$			± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS} = 10 \text{ V}$, $I_D = 1.5\text{A}$			0.14	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 25 \text{ V}$, $f = 1.0\text{MHz}$		250		pF
Output Capacitance	C_{OSS}			70		pF
Reverse Transfer Capacitance	C_{RSS}			15		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q_G	$V_{DS} = 48\text{V}$, $V_{GS} = 10\text{V}$, $I_D = 3.0\text{A}$, $I_G = 1\text{mA}$ (Note 1, 2)		11.3		nC
Gate-Source Charge	Q_{GS}			5.7		nC
Gate-Drain Charge	Q_{GD}			1.8		nC
Turn-ON Delay Time (Note 1)	$t_{D(ON)}$	$V_{DD} = 30\text{V}$, $V_{GS} = 10\text{V}$, $I_D = 3.0\text{A}$, $R_G = 25\Omega$ (Note 1, 2)		2.6		ns
Turn-ON Rise Time	t_R			15.2		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			3.4		ns
Turn-OFF Fall-Time	t_F			2.8		ns
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Maximum Body-Diode Continuous Current	I_S				3.0	A
Maximum Body-Diode Pulsed Current	I_{SM}				12	A
Diode Forward Voltage (Note 1)	V_{SD}	$I_S = 3.0\text{A}$, $V_{GS} = 0\text{V}$			1.4	V
Reverse Recovery Time (Note 1)	t_{rr}	$I_S = 3.0\text{A}$, $V_{GS} = 0\text{V}$,		40		nS
Reverse Recovery Charge	Q_{rr}	$di/dt = 100\text{A}/\mu\text{s}$		56		nC

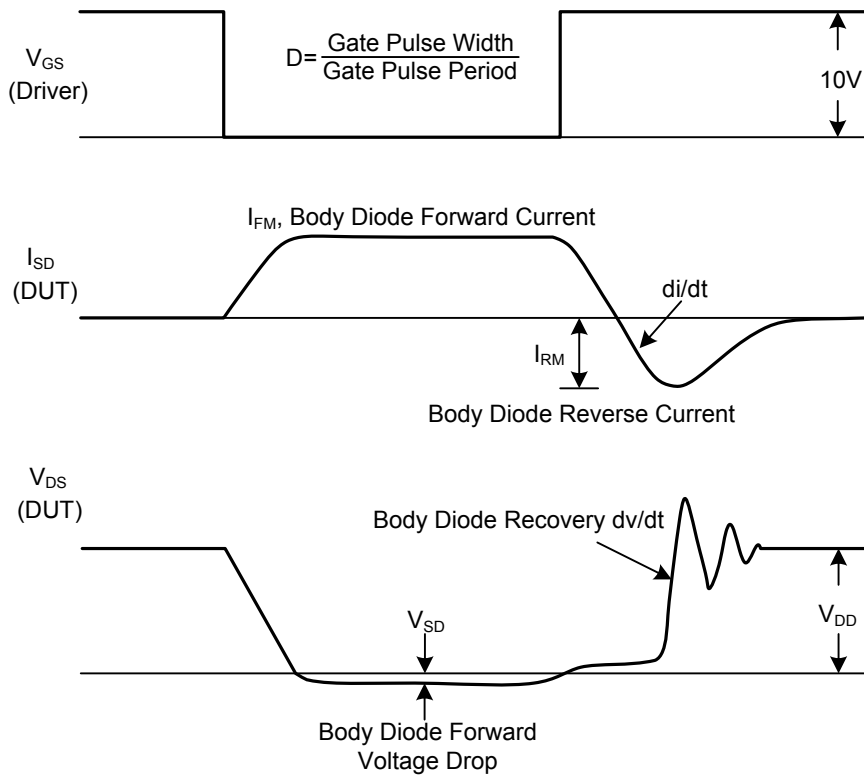
Notes: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS



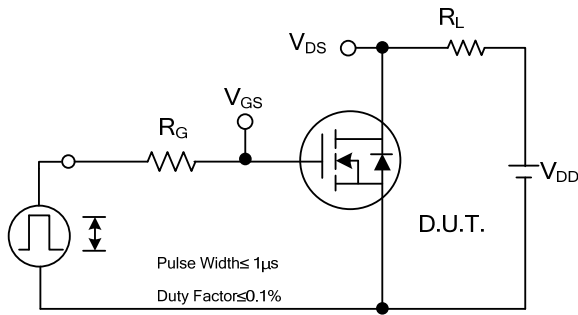
Peak Diode Recovery dv/dt Test Circuit



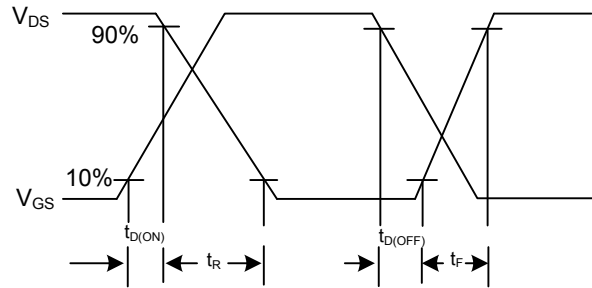
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

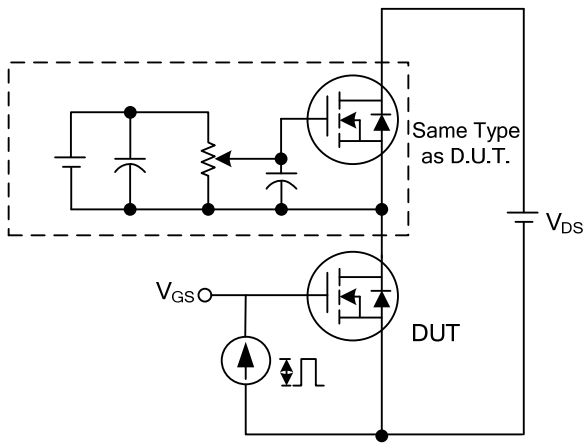
■ TEST CIRCUITS AND WAVEFORMS



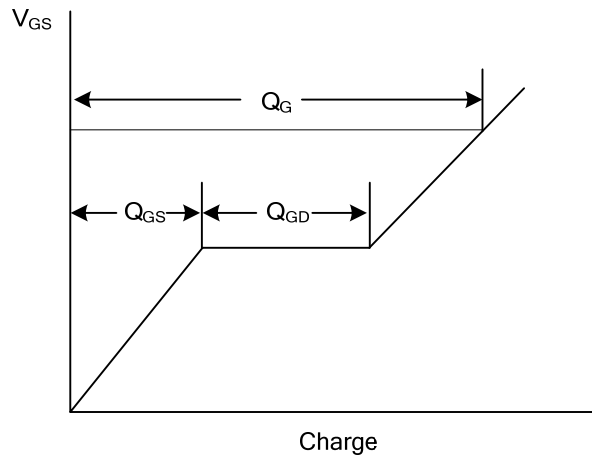
Switching Test Circuit



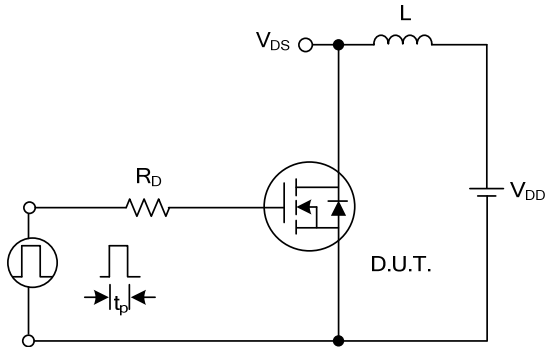
Switching Waveforms



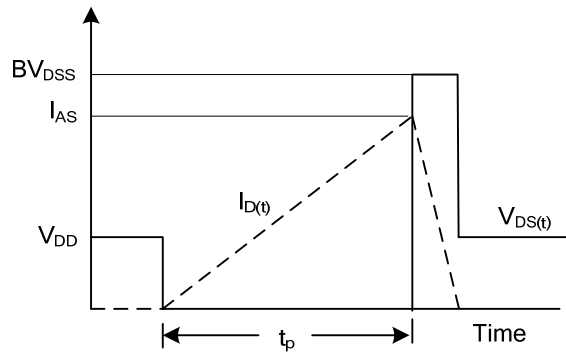
Gate Charge Test Circuit



Gate Charge Waveform

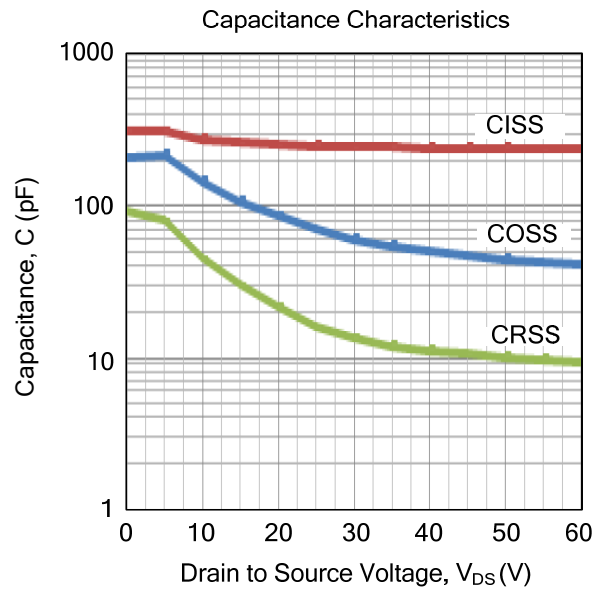
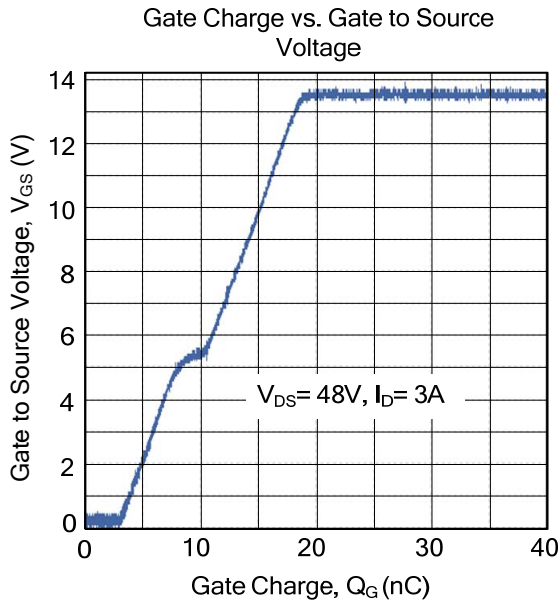


Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

■ TYPICAL CHARACTERISTICS



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