



UF5N07

Power MOSFET

5A, 70V N-CHANNEL ENHANCEMENT MODE POWER MOSFET

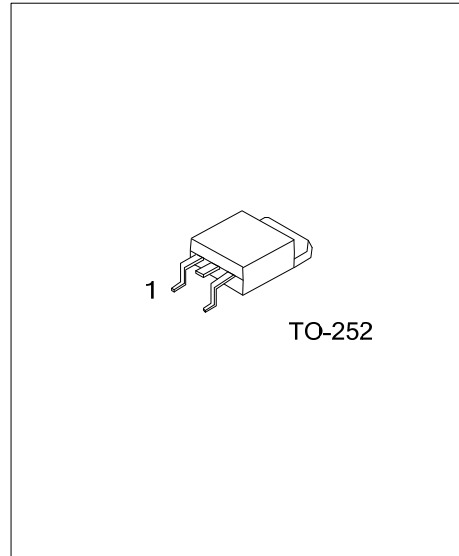
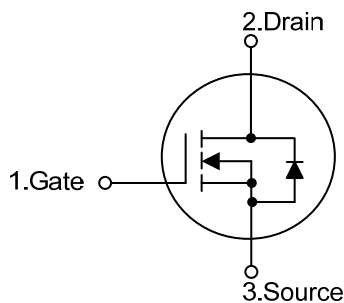
DESCRIPTION

The UTC **UF5N07** is a N-channel power MOSFET providing very low on-resistance. It has high efficiency and perfect cost-effectiveness. It can be generally applied in the commercial and industrial fields.

FEATURES

- * $R_{DS(ON)} < 0.2\Omega$ @ $V_{GS}=10V, I_D=2.5A$
- * Simple drive requirement

SYMBOL



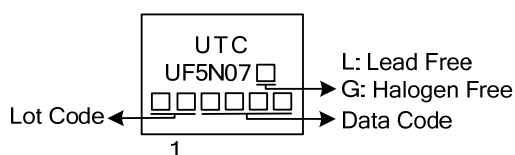
ORDERING INFORMATION

| Ordering Number | | Package | Pin Assignment | | | Packing |
|-----------------|---------------|---------|----------------|---|---|-----------|
| Lead Free | Halogen Free | | 1 | 2 | 3 | |
| UF5N07L-TN3-R | UF5N07G-TN3-R | TO-252 | G | D | S | Tape Reel |

Note: Pin Assignment: G: Gate D: Drain S: Source

| | |
|--|--|
| <p>UF5N07G-TN3-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p> | <p>(1) R: Tape Reel</p> <p>(2) TN3: TO-252</p> <p>(3) G: Halogen Free and Lead Free L: Lead Free</p> |
|--|--|

MARKING



■ ABSOLUTE MAXIMUM RATING ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

| PARAMETER | | SYMBOL | RATINGS | UNIT |
|------------------------------------|------------------------|-----------|------------|--------------------|
| Drain-Source Voltage | | V_{DSS} | 70 | V |
| Gate-Source Voltage | | V_{GSS} | ± 20 | V |
| Drain Current | Continuous | I_D | 5 | A |
| | Pulsed (Note 2) | I_{DM} | 15 | A |
| Avalanche Energy (Note 3) | Single Pulsed (Note 3) | E_{AS} | 11 | mJ |
| Peak Diode Recovery dv/dt (Note 4) | | dv/dt | 18 | V/ns |
| Power Dissipation | | P_D | 30 | W |
| Junction Temperature | | T_J | +150 | $^{\circ}\text{C}$ |
| Storage Temperature Range | | T_{STG} | -55 ~ +150 | $^{\circ}\text{C}$ |

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 0.1 \text{ mH}$, $I_{AS} = 15 \text{ A}$, $V_{DD} = 50 \text{ V}$, $R_G = 25 \Omega$, Starting $T_J = 25^{\circ}\text{C}$.

4. $I_{SD} \leq 5.0 \text{ A}$, $di/dt \leq 200 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J = 25^{\circ}\text{C}$.

■ THERMAL DATA

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---------------------|---------------|---------|-----------------------------|
| Junction to Ambient | θ_{JA} | 110 | $^{\circ}\text{C}/\text{W}$ |
| Junction to Case | θ_{JC} | 4.2 | $^{\circ}\text{C}/\text{W}$ |

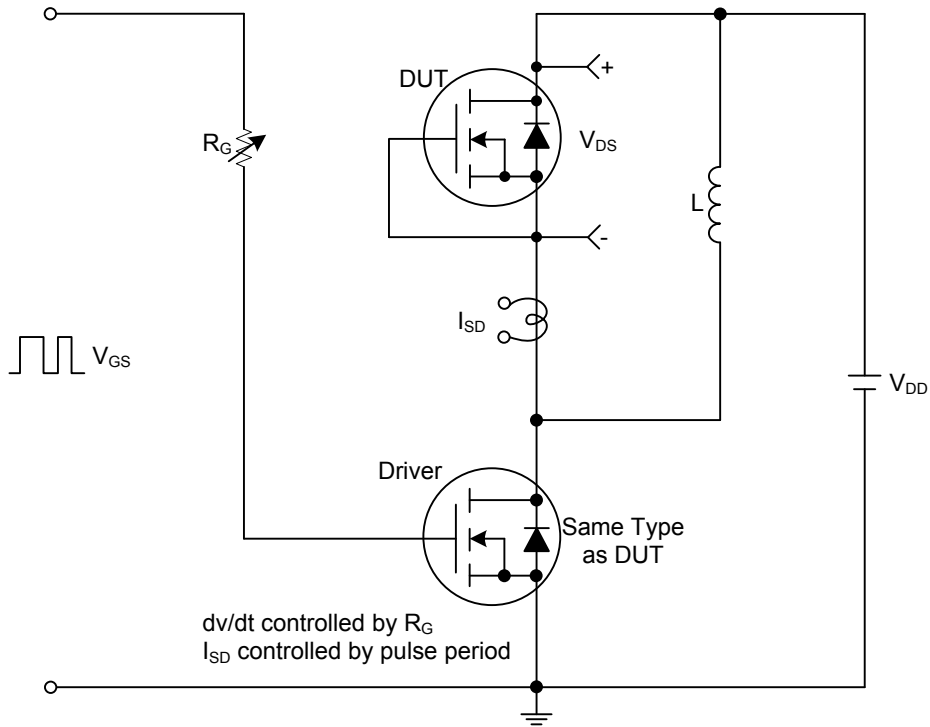
■ ELECTRICAL CHARACTERISTICS ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--------------|---|-----|------|-----------|---------------|
| OFF CHARACTERISTICS | | | | | | |
| Drain-Source Breakdown Voltage | BV_{DSS} | $V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$ | 70 | | | V |
| Drain-Source Leakage Current | I_{DSS} | $V_{DS}=70\text{V}$, $V_{GS}=0\text{V}$ | | | 10 | μA |
| Gate-Source Leakage Current | I_{GSS} | $V_{GS}=\pm 20\text{V}$ | | | ± 100 | nA |
| ON CHARACTERISTICS | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$ | 2.0 | | 4.0 | V |
| Drain to Source On-state Resistance | $R_{DS(ON)}$ | $V_{GS}=10\text{V}$, $I_D=2.5\text{A}$ | | | 0.2 | Ω |
| DYNAMIC PARAMETERS | | | | | | |
| Input Capacitance | C_{ISS} | $V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$ | | 250 | | pF |
| Output Capacitance | C_{OSS} | | | 55 | | pF |
| Reverse Transfer Capacitance | C_{RSS} | | | 10 | | pF |
| SWITCHING PARAMETERS | | | | | | |
| Total Gate Charge (Note 1) | Q_G | $V_{DS}=56\text{V}$, $V_{GS}=10\text{V}$, $I_D=5.0\text{A}$, $I_G=1\text{mA}$ (Note 1, 2) | | 11.3 | | nC |
| Gate Source Charge | Q_{GS} | | | 5.8 | | nC |
| Gate Drain Charge | Q_{GD} | | | 1.7 | | nC |
| Turn-ON Delay Time (Note 1) | $t_{D(ON)}$ | $V_{DD}=35\text{V}$, $V_{GS}=10\text{V}$, $I_D=5.0\text{A}$, $R_G=25\Omega$ (Note 1, 2) | | 2.4 | | ns |
| Turn-ON Rise Time | t_R | | | 15 | | ns |
| Turn-OFF Delay Time | $t_{D(OFF)}$ | | | 3.4 | | ns |
| Turn-OFF Fall-Time | t_F | | | 2.7 | | ns |
| SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS | | | | | | |
| Maximum Body-Diode Continuous Current | I_S | | | | 5 | A |
| Maximum Body-Diode Pulsed Current | I_{SM} | | | | 15 | A |
| Drain-Source Diode Forward Voltage (Note 1) | V_{SD} | $I_S=5.0\text{A}$, $V_{GS}=0\text{V}$ | | | 1.4 | V |
| Reverse Recovery Time (Note 1) | t_{rr} | $I_S=5.0\text{A}$, $V_{GS}=0\text{V}$, $dI/dt=100\text{A}/\mu\text{s}$ | | 40 | | ns |
| Reverse Recovery Charge | Q_{rr} | | | 110 | | nC |

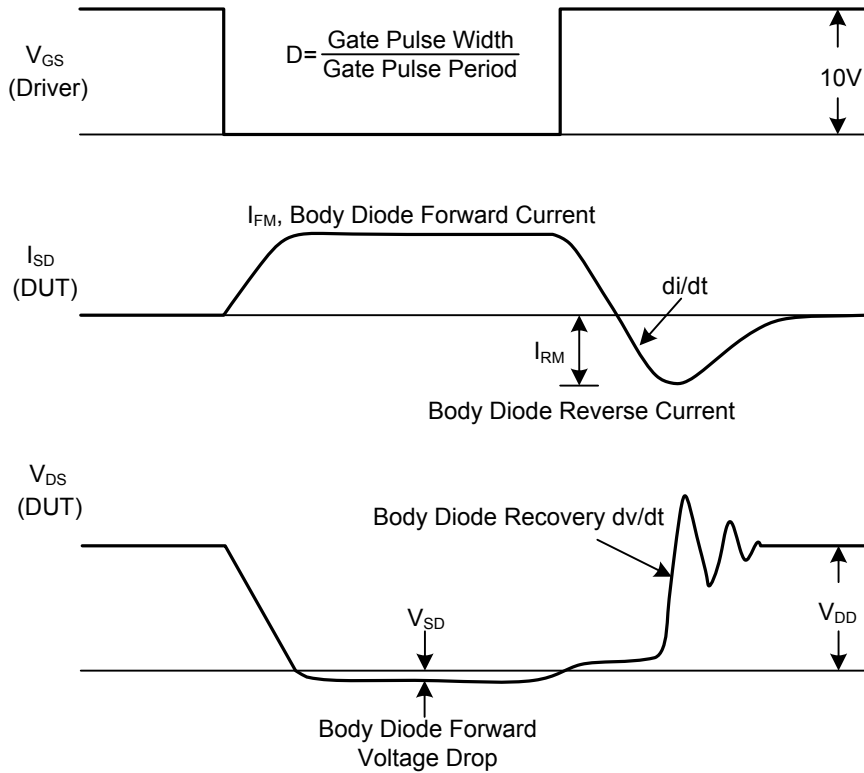
Notes: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating ambient temperature.

TEST CIRCUITS AND WAVEFORMS



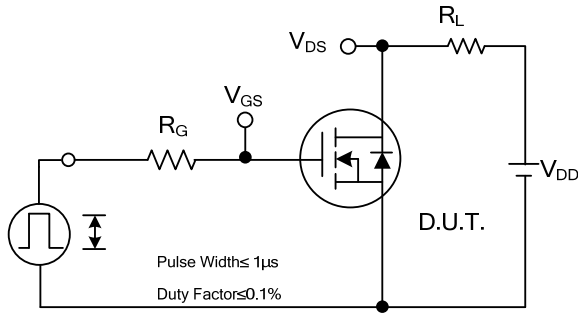
Peak Diode Recovery dv/dt Test Circuit



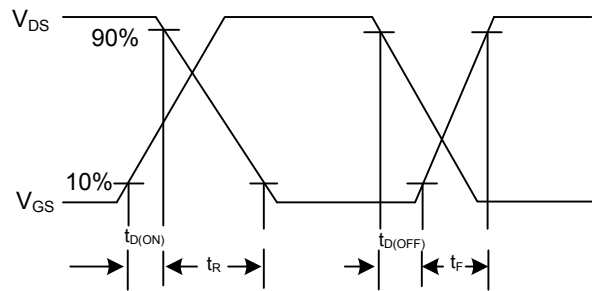
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

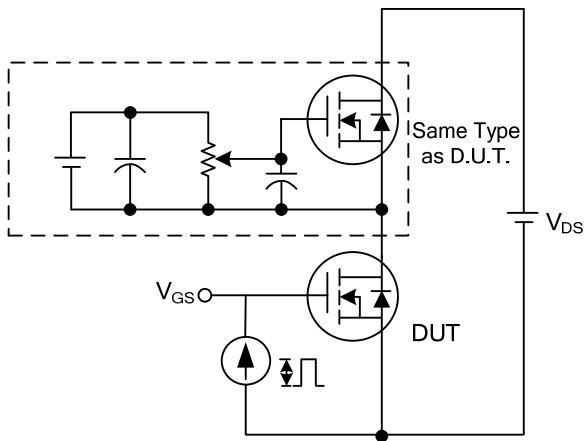
■ TEST CIRCUITS AND WAVEFORMS



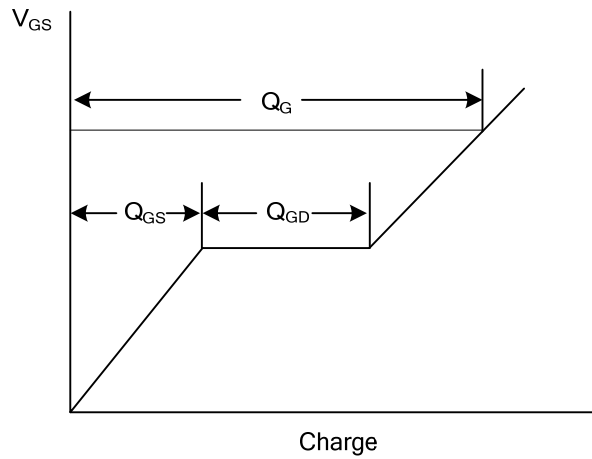
Switching Test Circuit



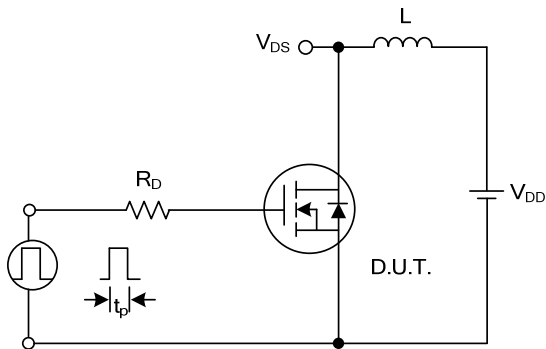
Switching Waveforms



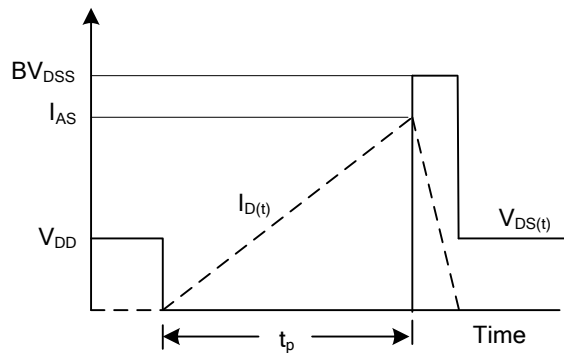
Gate Charge Test Circuit



Gate Charge Waveform

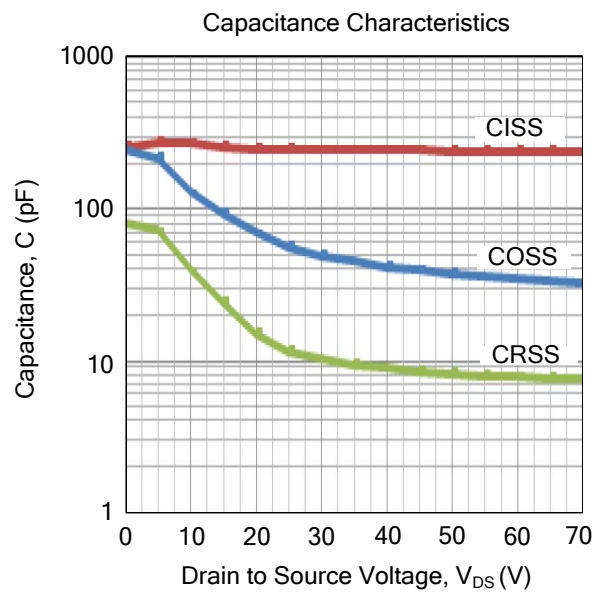
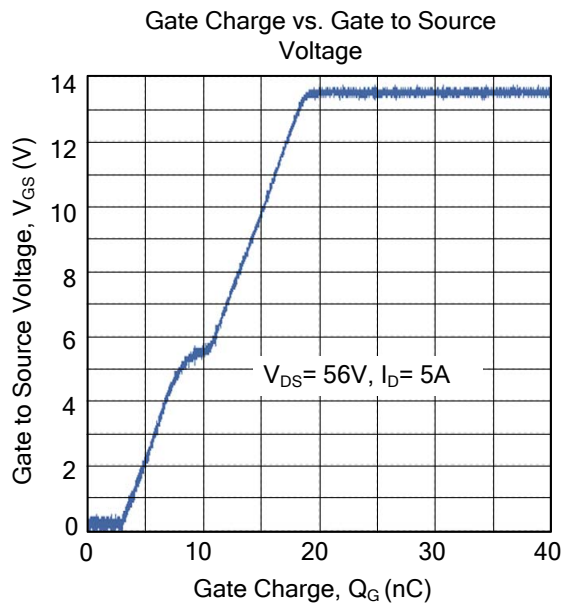


Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

TYPICAL CHARACTERISTICS



UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. UTC reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.