



5N40-MTQ

Preliminary

Power MOSFET

5A, 400V N-CHANNEL POWER MOSFET

DESCRIPTION

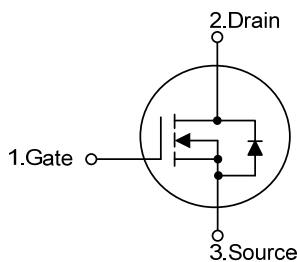
The UTC **5N40-MTQ** is a N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology specializes in allowing a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **5N40-MTQ** is universally applied in electronic lamp ballast based on half bridge topology and high efficient switched mode power supply.

FEATURES

- * $R_{DS(ON)} < 1.6\Omega @ V_{GS} = 10V, I_D = 2.5A$
- * High switching speed
- * 100% avalanche tested

SYMBOL



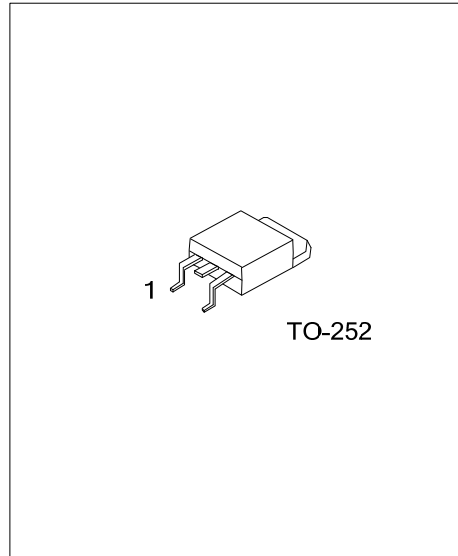
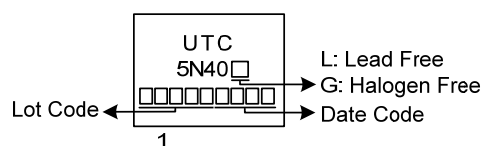
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
5N40L-TN3-R	5N40G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

5N40G-TN3-R	(1)Packing Type	(1) R: Tape Reel
	(2)Package Type	(2) TN3: TO-252
	(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	400	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous ($T_C=25^\circ\text{C}$)	I_D	5	A
	Pulsed (Note 2)	I_{DM}	10	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	116	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	4.9	V/ns
Power Dissipation		P_D	50	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L=18\text{mH}$, $I_{AS}=3.6\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\ \Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD}\leq 5.0\text{A}$, $di/dt\leq 100\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	110	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	2.5	$^\circ\text{C}/\text{W}$

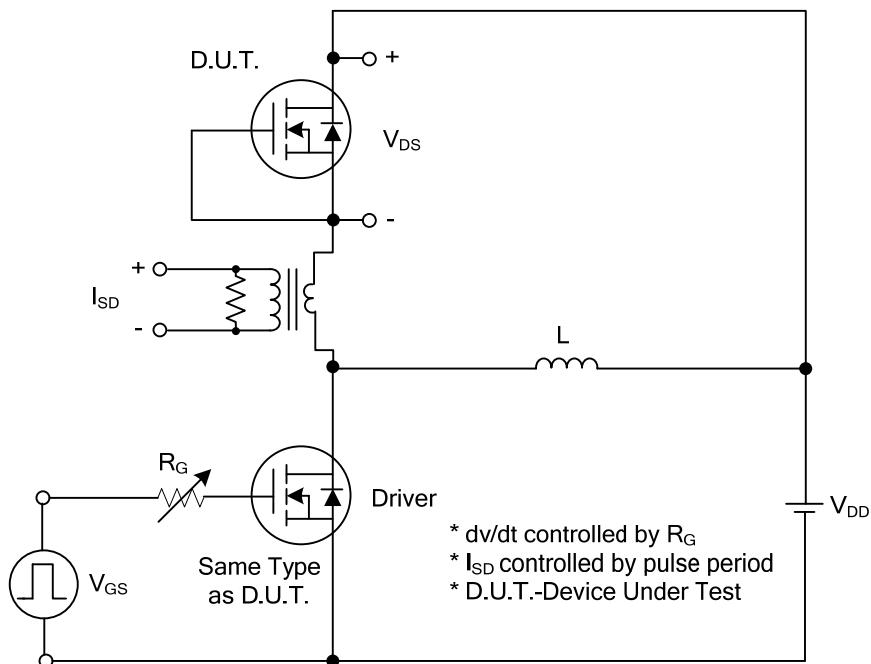
■ ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	400			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=400\text{V}$, $V_{GS}=0\text{V}$			10	μA
Gate- Source Leakage Current	I_{GSS}	Forward			+100	nA
		Reverse			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=2.5\text{A}$		1.3	1.6	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		400		pF
Output Capacitance	C_{OSS}			56		pF
Reverse Transfer Capacitance	C_{RSS}			4.5		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{DS}=100\text{V}$, $V_{GS}=10\text{V}$, $I_D=5.0\text{A}$, $I_G=1\text{mA}$ (Note 1, 2)		11.5		nC
Gate to Source Charge	Q_{GS}			4.9		nC
Gate to Drain Charge	Q_{GD}			2.3		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DS}=100\text{V}$, $V_{GS}=10\text{V}$, $I_D=5.0\text{A}$, $R_G=25\Omega$ (Note1,2)		6		ns
Rise Time	t_R			16.4		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			24.6		ns
Fall-Time	t_F			22		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_{SD}				5	A
Maximum Body-Diode Pulsed Current	I_{SM}				10	A
Drain-Source Diode Forward Voltage	V_{SD}	$I_S=5.0\text{A}$, $V_{GS}=0\text{V}$			1.5	V
Reverse Recovery Time (Note 1)	t_{rr}	$I_S=5.0\text{A}$, $V_{GS}=0\text{V}$, $dI_F/dt=100\text{A}/\mu\text{s}$		205		nS
Reverse Recovery Charge	Q_{rr}			1.34		μC

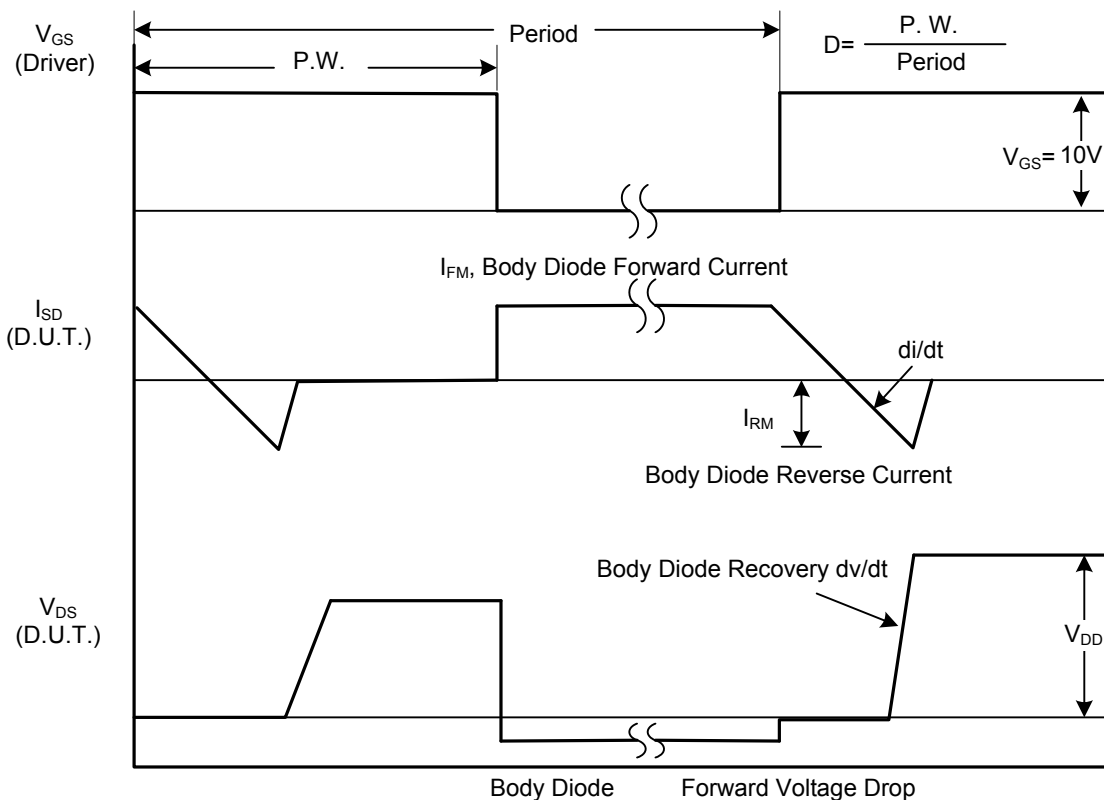
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

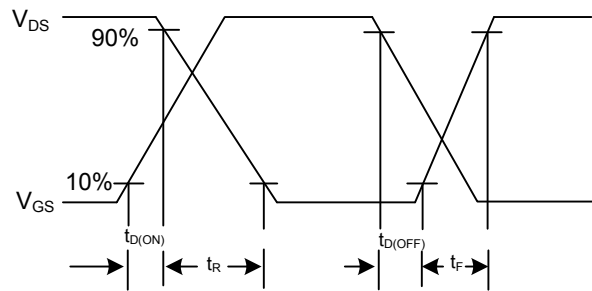
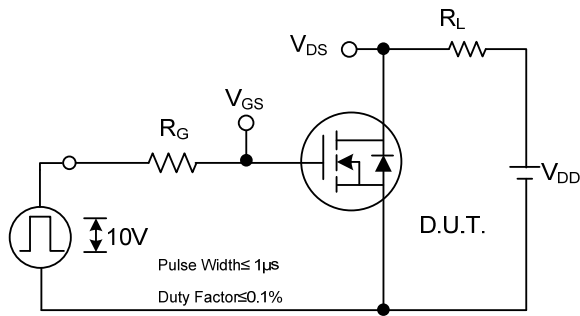


Peak Diode Recovery dv/dt Test Circuit



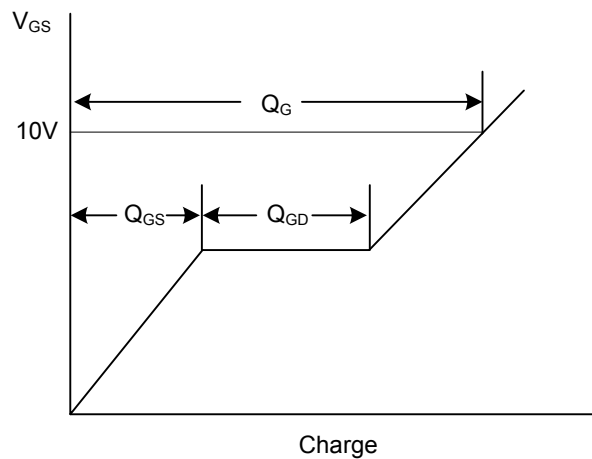
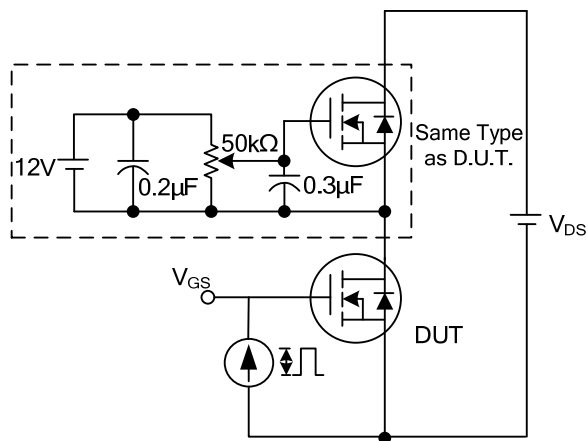
Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)



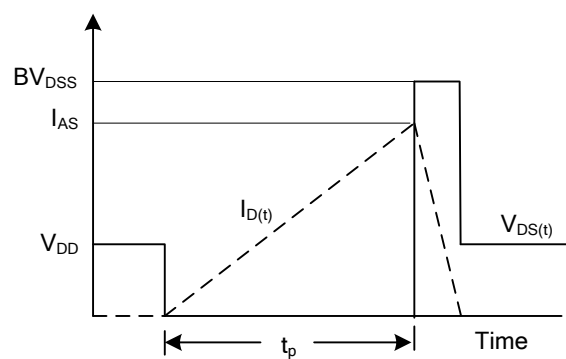
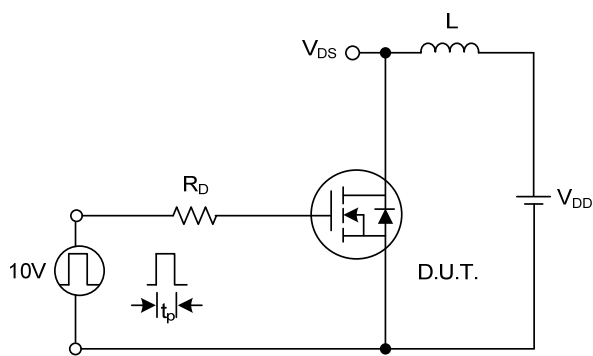
Switching Test Circuit

Switching Waveforms



Gate Charge Test Circuit

Gate Charge Waveform



Unclamped Inductive Switching Test Circuit

Unclamped Inductive Switching Waveforms

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