



U74HC273

CMOS IC

OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

DESCRIPTION

The **U74HC273** devices are positive-edge-triggered D-type flip-flops with a direct active low clear (CLR) input.

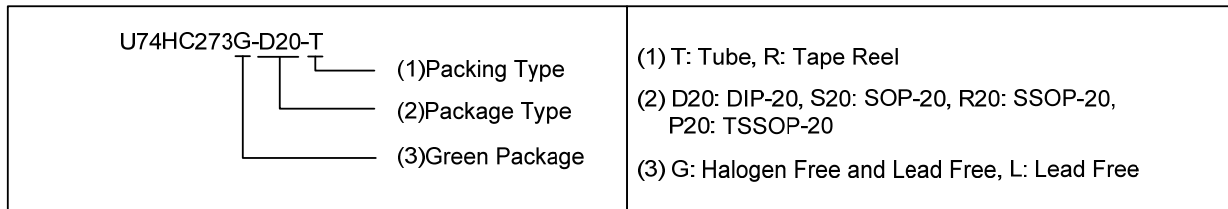
Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not related directly to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

FEATURES

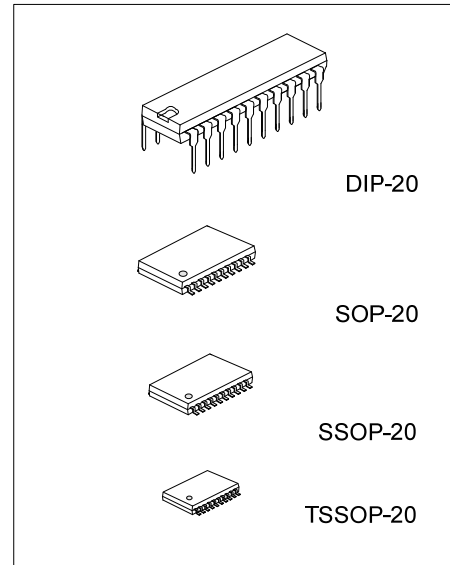
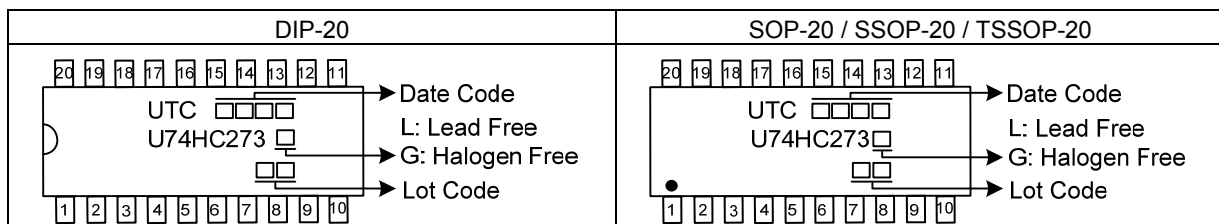
- * Wide Operating Voltage Range of 2V to 6V
- * Low Power Consumption, 80- μ A Maximum I_{CC}
- * Typical $t_{PD} = 12ns$
- * $\pm 4mA$ Output Drive at 5V
- * Low Input Current of 1 μ A Maximum
- * Contain Eight Flip-Flops With Single-Rail Outputs
- * Direct Clear Input
- * Individual Data Input to Each Flip-Flop

ORDERING INFORMATION

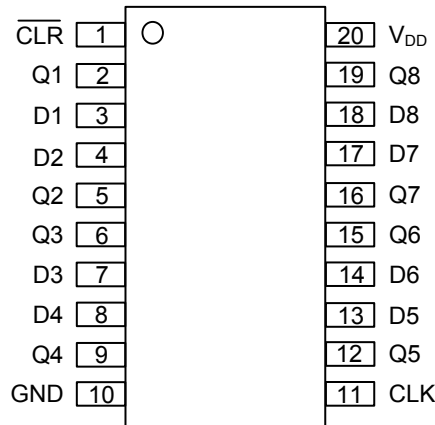
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC273L-D20-T	U74HC273G-D20-T	DIP-20	Tube
U74HC273L-S20-R	U74HC273G-S20-R	SOP-20	Tape Reel
U74HC273L-R20-R	U74HC273G-R20-R	SSOP-20	Tape Reel
U74HC273L-P20-R	U74HC273G-P20-R	TSSOP-20	Tape Reel



MARKING



■ PIN CONFIGURATION

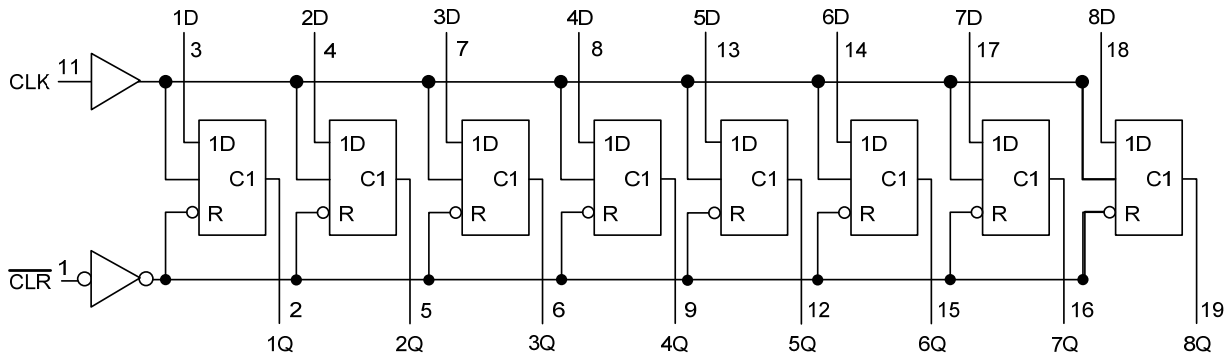


■ FUNCTION TABLE

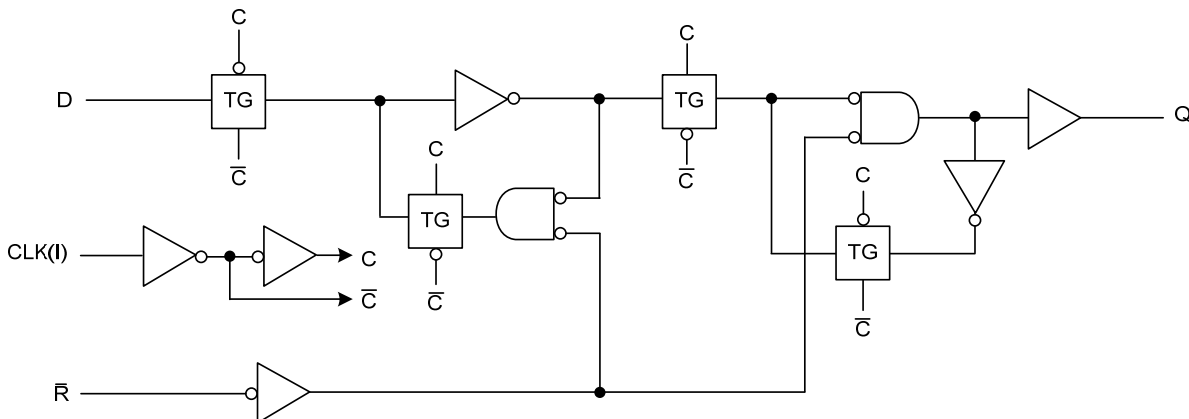
INPUTS			OUTPUT
$\overline{\text{CLR}}$	CLK	D	Q
L	X	X	L
H	\uparrow	H	H
H	\uparrow	L	L
H	L	X	Q_0

H = High voltage level ; L = Low voltage level ; X = Don't care

■ FUNCTIONAL BLOCK DIAGRAM



■ LOGIC DIAGRAM, EACH FLIP-FLOP (POSITIVE LOGIC)



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V _{CC}		-0.5 ~ 7.0	V
V _{CC} or GND Current	I _{CC}		±50	mA
Continuous Output Current	I _{OUT}	V _{OUT} =0 ~ V _{CC}	±25	mA
Input Clamp Current	I _{IK}	V _{IN} <0 or V _{IN} <V _{CC}	±20	mA
Output Clamp Current	I _{OK}	V _{IN} <0 or V _{OUT} >V _{CC}	±20	mA
Storage Temperature Range	T _{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V _{CC}		2	5	6	V
High-Level Input Voltage	V _{IH}	V _{CC} =2V	1.5			V
		V _{CC} =4.5V	3.15			V
		V _{CC} =6V	4.2			V
Low-Level Input Voltage	V _{IL}	V _{CC} =2V			0.5	V
		V _{CC} =4.5V			1.35	V
		V _{CC} =6V			1.8	V
Input Voltage	V _{IN}		0		V _{CC}	V
Output Voltage	V _{OUT}		0		V _{CC}	V
Input Transition Rise or Fall Rate	t _R , t _F	V _{CC} =2V			1000	ns
		V _{CC} =4.5V			500	ns
		V _{CC} =6V			400	ns
Operating Temperature	T _A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
High-Level Output Voltage	V _{OH}	V _{CC} =2V, I _{OH} =-20μA	1.9	1.998		1.9			V
		V _{CC} =4.5V, I _{OH} =-20μA	4.4	4.499		4.4			V
		V _{CC} =6V, I _{OH} =-20μA	5.9	5.999		5.9			V
		V _{CC} =4.5V, I _{OH} =-4mA	3.98	4.3		3.7			V
		V _{CC} =6V, I _{OH} =-5.2mA	5.48	5.8		5.2			V
Low-Level Output Voltage	V _{OL}	V _{CC} =2V, I _{OL} =20μA		0.002	0.1			0.1	V
		V _{CC} =4.5V, I _{OL} =20μA		0.001	0.1			0.1	V
		V _{CC} =6V, I _{OL} =20μA		0.001	0.1			0.1	V
		V _{CC} =4.5V, I _{OL} =4mA		0.17	0.26			0.4	V
		V _{CC} =6V, I _{OL} =5.2mA		0.15	0.26			0.4	V
Input Leakage Current	I _{I(LEAK)}	V _{CC} =6V, V _I =V _{CC} or 0		±0.1	±100			±100	μA
Quiescent Supply Current	I _{CC}	V _{CC} =6V, V _I =V _{CC} or 0, I _{OUT} =0			8			160	μA

■ SWITCHING CHARACTERISTICS ($C_L=50\text{pF}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A=25^\circ\text{C}$			$T_A=-40\sim+125^\circ\text{C}$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Maximum clock pulse frequency	f_{MAX}	$V_{\text{CC}}=2.0\text{V}$	5	11		4			MHz
		$V_{\text{CC}}=4.5\text{V}$	27	50		20			MHz
		$V_{\text{CC}}=6.0\text{V}$	32	60		24			MHz
Propagation delay from input ($\overline{\text{CLR}}$) to output (Any)	t_{PHL}	$V_{\text{CC}}=2.0\text{V}$		55	160			225	ns
		$V_{\text{CC}}=4.5\text{V}$		15	32			45	ns
		$V_{\text{CC}}=6.0\text{V}$		12	27			38	ns
Propagation delay from input (CLK) to output (Any)	t_{PD}	$V_{\text{CC}}=2.0\text{V}$		56	160			225	ns
		$V_{\text{CC}}=4.5\text{V}$		15	32			45	ns
		$V_{\text{CC}}=6.0\text{V}$		13	27			38	ns
Propagation delay to output (Any)	t_t	$V_{\text{CC}}=2.0\text{V}$		38	75			110	ns
		$V_{\text{CC}}=4.5\text{V}$		8	15			22	ns
		$V_{\text{CC}}=6.0\text{V}$		6	13			19	ns

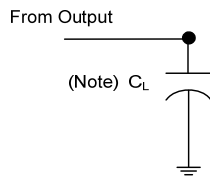
■ TIMING REQUIREMENTS (Input: $t_R, t_F \leq 2.5\text{ns}$; $\text{PRR} \leq 1\text{MHz}$)

PARAMETER		SYMBOL	Conditions	$T_A=25^\circ\text{C}$			$T_A=-40\sim+125^\circ\text{C}$			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Clock frequency		f_{CLOCK}	$V_{\text{CC}}=2\text{V}$			5			4	MHz
			$V_{\text{CC}}=4.5\text{V}$			27			20	MHz
			$V_{\text{CC}}=6\text{V}$			32			24	MHz
Pulse duration	CLK high or low	t_w	$V_{\text{CC}}=2\text{V}$		80		120			ns
			$V_{\text{CC}}=4.5\text{V}$		16		24			ns
			$V_{\text{CC}}=6\text{V}$		14		20			ns
	$\overline{\text{CLR}}$ low		$V_{\text{CC}}=2\text{V}$		80		120			ns
			$V_{\text{CC}}=4.5\text{V}$		16		24			ns
			$V_{\text{CC}}=6\text{V}$		14		20			ns
Setup time before CLK \uparrow	Data	t_{SU}	$V_{\text{CC}}=2\text{V}$		100		120			ns
			$V_{\text{CC}}=4.5\text{V}$		20		24			ns
			$V_{\text{CC}}=6\text{V}$		17		20			ns
	$\overline{\text{CLR}}$ inactive		$V_{\text{CC}}=2\text{V}$		100		120			ns
			$V_{\text{CC}}=4.5\text{V}$		20		24			ns
			$V_{\text{CC}}=6\text{V}$		17		20			ns
Hold time ,data after CLK \uparrow		t_H	$V_{\text{CC}}=2\text{V}$		0		-6			ns
			$V_{\text{CC}}=4.5\text{V}$		0		-2			ns
			$V_{\text{CC}}=6\text{V}$		0		-2			ns

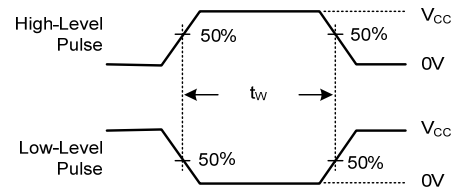
■ OPERATING CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C_I	$V_{\text{CC}}=2\text{V}\sim 6\text{V}$		3	10	pF
Power Dissipation Capacitance per flip-flop	C_{PD}	No load.		35		pF

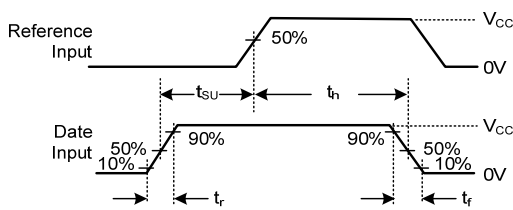
■ TEST CIRCUIT AND WAVEFORMS



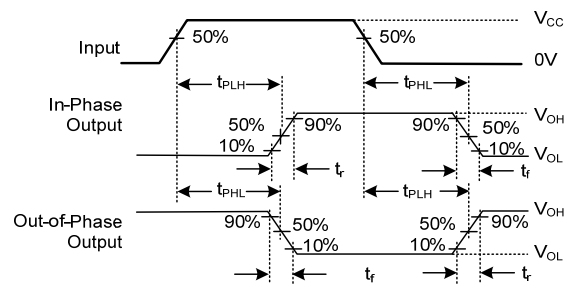
Load Circuit



Voltage Waveforms Pulse Durations



Voltage Waveforms Setup and Hold Times



Voltage Waveforms Propagation Delay and Output Transition Times

- Notes:
1. C_L includes probe and jig capacitance.
 2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O = 50\Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 3. For clock inputs, fmax is measured when the input duty cycle is 50%.
 4. The outputs are measured one at a time with one input transition per measurement.

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