



# U74LVC540

CMOS IC

## OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

### DESCRIPTION

The **U74LVC540** octal buffer/driver is designed for 1.65V to 3.6V  $V_{CC}$  operation.

These devices are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package that facilitate printed circuit board layout.

### FEATURES

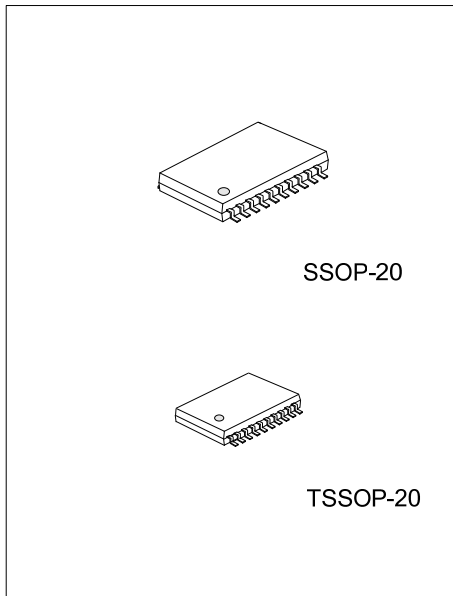
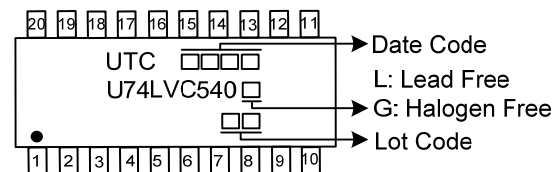
- \* Wide Operating Voltage Range of 1.65V to 3.6V
- \* Inputs Accept Voltages to 5.5V
- \* Max tpd of 5.3ns at 3.3V
- \* Typical VOLP (Output Ground Bounce) < 0.8 V at  $V_{CC}=3.3$  V,  $T_A=25^\circ\text{C}$
- \* Typical VOHV (Output  $V_{OH}$  Undershoot) > 2 V at  $V_{CC}=3.3$  V,  $T_A=25^\circ\text{C}$
- \* Support Mixed-Mode Signal Operation on All Ports (5V Input/Output Voltage With 3.3V  $V_{CC}$ )
- \*  $I_{OFF}$  Supports Partial-Power-Down Mode Operation

### ORDERING INFORMATION

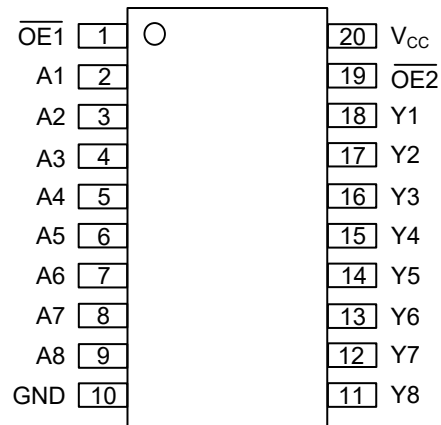
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC540L-R20-R	U74LVC540G-R20-R	SSOP-20	Tape Reel
U74LVC540L-P20-R	U74LVC540G-P20-R	TSSOP-20	Tape Reel

<p>U74LVC540G-R20-R</p>	<p>(1) R: Tape Reel                  (2) R20: SSOP-20, P20: TSSOP-20                  (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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### MARKING



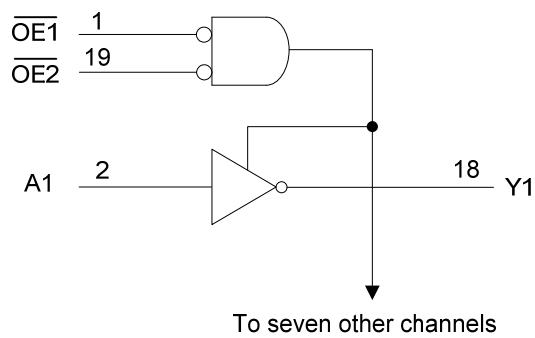
■ PIN CONFIGURATION



■ FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

■ LOGIC DIAGRAM (positive logic)



## ■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	$V_{CC}$		-0.5 ~ +6.5	V
Input Voltage	$V_{IN}$		-0.5 ~ +6.5	V
Output Voltage (Note 2)	$V_{OUT}$	Output in the High or Low State	-0.5 ~ +6.5	V
		High-Impedance or Power-Off State	-0.5 ~ + $V_{CC}$ +0.5	V
Continuous Output Current	$I_{OUT}$		±50	mA
		$V_{CC}$ or GND	±100	mA
Input Clamp Current	$I_{IK}$	$V_{IN} < 0V$	-50	mA
Output Clamp Current	$I_{OK}$	$V_{OUT} < 0V$	-50	mA
Storage Temperature Range	$T_{STG}$		-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.  
 2. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

## ■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	$V_{CC}$	Operating	1.65		3.6	V
		Data Retention Only	1.5			V
Input Voltage	$V_{IN}$		0		5.5	V
Output Voltage	$V_{OUT}$	3-State	0		5.5	V
		High or Low State	0		$V_{CC}$	V
Operating Temperature	$T_A$		-40		+125	°C

## ■ ELECTRICAL CHARACTERISTICS ( $T_A=25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level Input Voltage	$V_{IH}$	$V_{CC}=1.65V\sim 1.95V$	$0.65 \times V_{CC}$			V
		$V_{CC}=2.3V\sim 2.7V$	1.7			V
		$V_{CC}=2.7V\sim 3.6V$	2			V
Low-level Input Voltage	$V_{IL}$	$V_{CC}=1.65V\sim 1.95V$			$0.35 \times V_{CC}$	V
		$V_{CC}=2.3V\sim 2.7V$			0.7	V
		$V_{CC}=2.7V\sim 3.6V$			0.8	V
High-Level Output Voltage	$V_{OH}$	$V_{CC}=1.65V\sim 3.6V, I_{OH}=-100\mu A$	$V_{CC}-0.2$			V
		$V_{CC}=1.65V, I_{OH}=-4mA$	1.2			V
		$V_{CC}=2.3V, I_{OH}=-8mA$	1.7			V
		$V_{CC}=2.7V$	2.2			V
		$V_{CC}=3V$	2.4			V
		$V_{CC}=3V, I_{OH}=-24mA$	2.2			V
Low-Level Output Voltage	$V_{OL}$	$V_{CC}=1.65V\sim 3.6V, I_{OL}=100\mu A$			0.2	V
		$V_{CC}=1.65V, I_{OL}=4mA$			0.45	V
		$V_{CC}=2.3V, I_{OL}=8mA$			0.7	V
		$V_{CC}=2.7V, I_{OL}=12mA$			0.4	V
		$V_{CC}=3V, I_{OL}=24mA$			0.55	V

### ■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=3.6V, V_{IN}=0\sim 5.5V$			$\pm 5$	$\mu A$
Power OFF Leakage Current	$I_{off}$	$V_{CC}=0V, V_{IN}$ or $V_{OUT}=5.5V$			$\pm 10$	$\mu A$
OFF-state output current	$I_{OZ}$	$V_{CC}=3.6V, V_{OUT}=0$ to $5.5V$			$\pm 10$	$\mu A$
Quiescent Supply Current	$I_{CC}$	$V_{CC}=3.6V, V_{IN}=V_{CC}$ or GND			10	$\mu A$
		$I_{OUT}=0, 3.6V \leq V_I \leq 5.5V$			10	$\mu A$
Additional Quiescent Supply Current Per Input Pin	$\Delta I_{CC}$	$V_{CC}=2.7V\sim 3.6V$ , One input at $V_{CC}-0.6V$ , Other inputs at $V_{CC}$ or GND			500	$\mu A$
Input Capacitance	$C_I$	$V_{CC}=3.3V, V_{IN}=GND$ or $V_{CC}$		4		pF
Output Capacitance	$C_O$	$V_{CC}=3.3V, V_{OUT}=GND$ or $V_{CC}$		5.5		pF

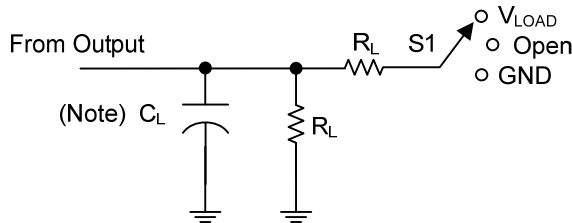
### ■ SWITCHING CHARACTERISTICS ( $T_A=25^\circ C$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (A) to output(Y)	$t_{PD}$	$V_{CC}=1.8V \pm 0.15V$	1		16.4	ns
		$V_{CC}=2.5V \pm 0.2V$	1		7.8	ns
		$V_{CC}=2.7V$	1		7.1	ns
		$V_{CC}=3.3V \pm 0.3V$	1.4		5.3	ns
Propagation delay from input ( $\overline{OE}$ ) to output(Y)	$t_{en}$	$V_{CC}=1.8V \pm 0.15V$	1		16.5	ns
		$V_{CC}=2.5V \pm 0.2V$	1		10.5	ns
		$V_{CC}=2.7V$	1		8	ns
		$V_{CC}=3.3V \pm 0.3V$	1.1		6.6	ns
Propagation delay from input ( $\overline{OE}$ ) to output(Y)	$t_{dis}$	$V_{CC}=1.8V \pm 0.15V$	1		15.9	ns
		$V_{CC}=2.5V \pm 0.2V$	1		9	ns
		$V_{CC}=2.7V$	1		8.2	ns
		$V_{CC}=3.3V \pm 0.3V$	1.8		7.4	ns
Propagation delay	$t_{SK(O)}$	$V_{CC}=3.3V \pm 0.3V$			1	ns

### ■ OPERATING CHARACTERISTICS ( $f=10MHz, T_A=25^\circ C$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Power Dissipation Capacitance	Output Enabled	$V_{CC}=1.8V$		63		pF	
		$V_{CC}=2.5V$		56		pF	
		$V_{CC}=3.3V$		31		pF	
	Output Disabled	$V_{CC}=1.8V$			3		pF
		$V_{CC}=2.5V$			3		pF
		$V_{CC}=3.3V$			3		pF

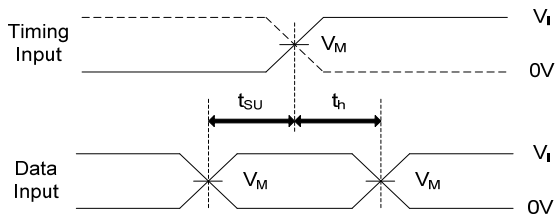
## TEST CIRCUIT AND WAVEFORMS



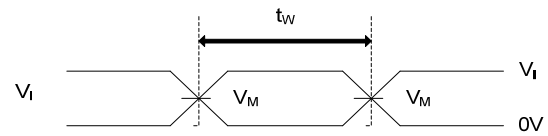
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

Note:  $C_L$  includes probe and jig capacitance.

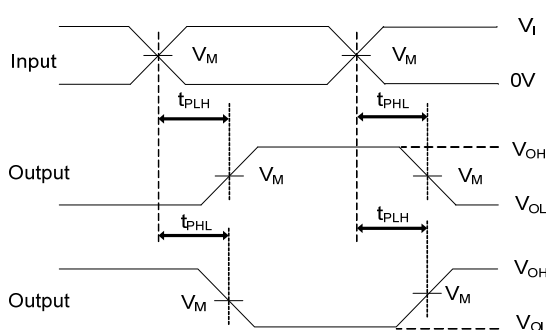
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_R/t_F$					
$1.8V \pm 0.15V$	$V_{CC}$	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	30pF	1k $\Omega$	0.15V
$2.5V \pm 0.2V$	$V_{CC}$	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	30pF	500 $\Omega$	0.15V
2.7V	2.7V	$\leq 2.5ns$	1.5V	6V	50pF	500 $\Omega$	0.3V
$3.3V \pm 0.3V$	2.7V	$\leq 2.5ns$	1.5V	6V	50pF	500 $\Omega$	0.3V



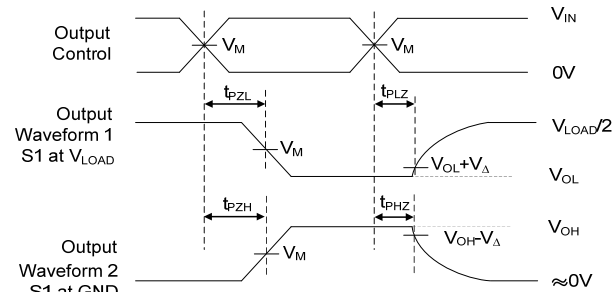
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

Notes: 1.  $C_L$  includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10MHz$ ,  $Z_O = 50\Omega$ .

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