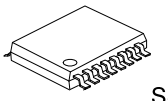
LOW POWER 4 STAGE FET BIAS CONTROLLER



SSOP-16
(150mil)

QFN-16(3x3)

■ DESCRIPTION

The UTC **L8402** is designed to bias the MOSFETs that are commonly used in LNBs that can implies minimum external components requires.

The UTC **L8402**, provide four FETs bias control respectively. By adjusting two external resistors, it can change the FET's bias current to optimize the satellite receiver front end block performances.

As an additional feature the Rcal pins can also be used as logic inputs to disable pairs of FETs as part of a power management scheme or simply an alternative to LNA switching. Driven to a logic high (>3.0V), the inputs disable their associated FET bias stages by switching gate feeds to 2.5V and drain feeds open circuit.

It generates the required negative voltage to bias the gate of FETs, and internally provides protection circuit that can protect the FET devices during supply voltage transient. So it is very popular in satellite receiver front end block.

■ FEATURES

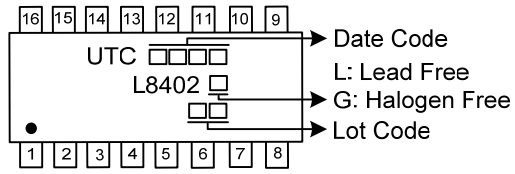
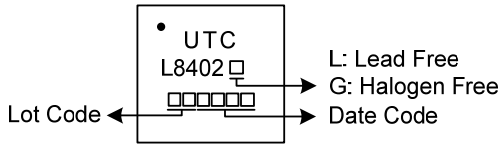
* Can Bias up to 4 FETs
* Wide supply voltage range: 3V~8V
* Low quiescent supply current, 1mA typical
* FET drain voltages set at 2.0V
* Adjustable FET device operating current
* FET drain voltages and currents held stable over temperature and V_{CC} variations
* Built in FET device protection circuit
* Low external component count

■ ORDERING INFORMATION

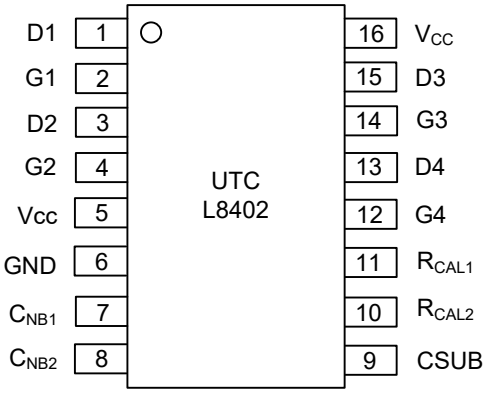
Ordering Number		Package	Packing
Lead Free	Halogen Free		
L8402L-R16-R	L8402G-R16-R	SSOP-16	Tape Reel
L8402L-Q16-3030-R	L8402G-Q16-3030-R	QFN-16(3×3)	Tape Reel

L8402G-S16-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) R16: SSOP-16, Q16-3030: QFN-16(3×3) (3) G: Halogen Free and Lead Free, L: Lead Free

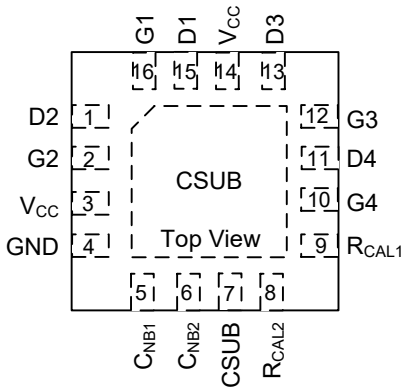
■ MARKING

SSOP-16	QFN-16(3×3)
	

■ PIN CONFIGURATION



SSOP-16

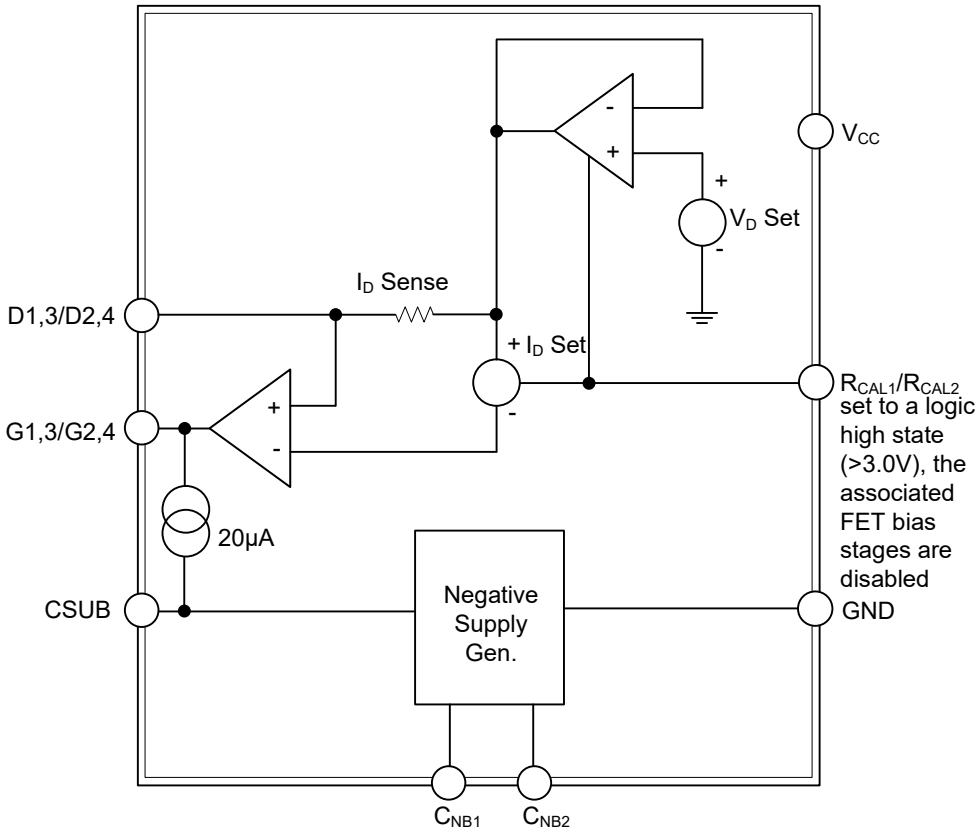


QFN-16(3×3)

■ PIN DESCRIPTION

PIN NO.		PIN NAME	DESCRIPTION
SSOP-16	QFN-16(3×3)		
1	15	D1	To D of FET 1
2	16	G1	To G of FET 1
3	1	D2	To D of FET 2
4	2	G2	To G of FET 2
5	3	V_{CC}	Power supply
6	4	GND	GND
7	5	C_{NB1}	Connect an external cap to C_{NB1}
8	6	C_{NB2}	Connect an external cap to C_{NB2}
9	7	CSUB	Connect an external cap to produce -2.5V
10	8	R_{CAL2}	Setting Id2/4 to 10mA
11	9	R_{CAL1}	Setting Id1/3 to 10mA
12	10	G4	To G of FET 4
13	11	D4	To D of FET 4
14	12	G3	To G of FET 3
15	13	D3	To D of FET 3
16	14	V_{CC}	Power supply (Pin 14 needs to be powered for the device to function)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.6 ~ +10	V
Supply Current	I_{CC}	80	mA
Power Dissipation	P_D	500	mW
Operating Temperature Range	T_{OPR}	-40 ~ +100	°C
Storage Temperature Range	T_{STG}	-40 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

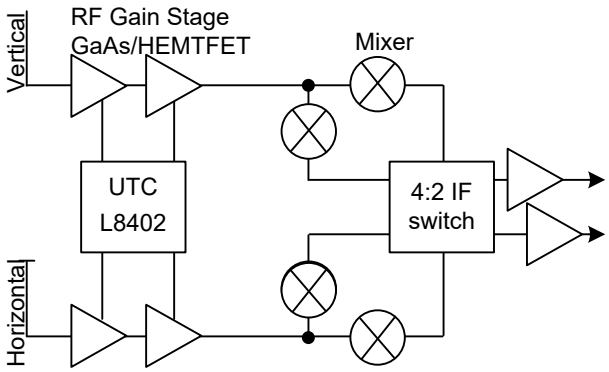
■ ELECTRICAL CHARACTERISTICS

(Measured at T_{AMB}=25°C, V_{CC}=3.3V (Note 1), $R_{CAL}1$=$R_{CAL}2$=39kΩ (setting I_D to 10mA) unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range (Note 1)	V_{CC}		3.0		8.0	V
Supply Current	I_{CC}	I_{D1}=I_{D2}=I_{D3}=I_{D4}=0		1	4.0	mA
	$I_{CC(L)}$	I_{D1}=I_{D2}=I_{D3}=I_{D4}=10mA		42	44	mA
Substrate Voltage	V_{CSUB}	I_{CSUB}=0	-3.0	-2.65	-2.0	V
	$V_{CSUB(L)}$	I_{CSUB}=-200μA		-2.55	-2.0	V
Oscillator Frequency	F_{OSC}		100		600	kHz
Gate Characteristics						
Gate (G1 to G4)						
Current Range	I_G		-100		+500	μA
Voltage Low	$V_{G(L)}$	I_D=12mA, I_G=-10μA	-3.0	-2.5	-2.0	V
Voltage High	$V_{G(H)}$	I_D=8mA, I_G=0	0	0.6	1.0	V
Voltage Disabled	$V_{G(DIS)}$	I_D=0, I_G=-10μA, V_{RCAL}=3.0V	-3.0	-2.5	-2.0	V
Drain Characteristics						
Drain (D1 to D4)						
Current Range	I_D		0		15	mA
Current Operating	$I_{D(OP)}$	Standard Application Circuit	8	10	12	mA
Current Disabled	$I_{D(DIS)}$	V_D=0, V_{RCAL}=3.0V			10	μA
Voltage Operating	$V_{D(OP)}$	I_D=10mA	1.8	2.0	2.2	V
Delta I_D vs. V_{CC}	dI_D/dV_{CC}	V_{CC}=3.3~8.0V		1.2		%/V
Delta V_D vs. V_{CC}	dV_D/dV_{CC}	V_{CC}=3.3~8.0V		0.15		%/V
R_{CAL} (1 and 2)						
Disable Threshold	$V_{RCAL(DIS)}$		1.8	2.5	3.0	V
Input Current	$I_{RCAL(DIS)}$			3.0	10	μA
Output Noise						
Drain Voltage	$V_{D(NOISE)}$	$C_{GATE-GND}$=10nF, $C_{DRAIN-GND}$=10nF		0.02		Vpk-pk
Gate Voltage	$V_{G(NOISE)}$	$C_{GATE-GND}$=10nF, $C_{DRAIN-GND}$=10nF		0.005		Vpk-pk

Notes: 1. The two Vcc pins are internally connected, pin 14 needs to be powered for the device to function.
2. ESD sensitive, handling precautions are recommended.
3. The negative bias supply voltage includes an internal OSC and two 47nF external cap.
4. The QFN-16(3×3) package exposed pad must either be connected to Csub or left open circuit.
5. The characteristics are measured using two external reference resistors R_{CAL1} and R_{CAL2} of value 39kΩ, wired from pins $R_{CAL1/2}$ to ground. Resistor R_{CAL1} sets the drain current of FETs 1 and 3, resistor R_{CAL2} sets the drain currents of FETs 2 and 4.
6. FETs and gate and drain capacitor of value 10nF make the most contribution to noise voltage, and noise voltages need not to measure in production.

■ LNB SYSTEM DIAGRAM



■ TYPICAL APPLICATION CIRCUIT

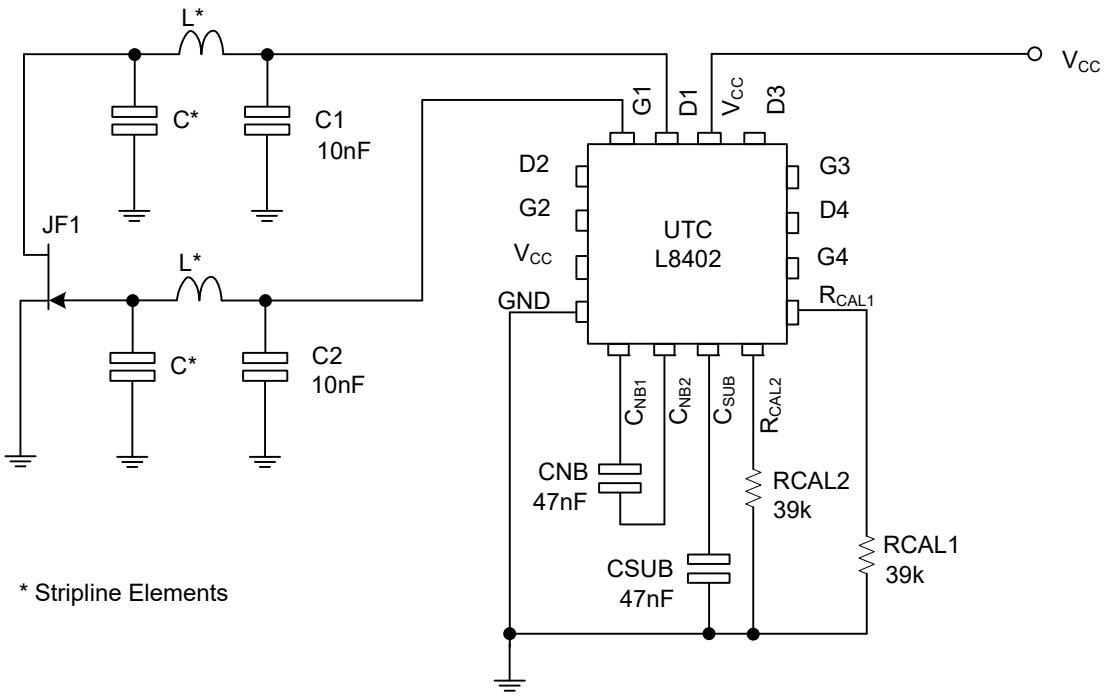


Fig. 2

Applications Information

It is application circuit of UTC **L8402** in figure 2, the bias circuits is stable fully in -40°C ~100°C.

CNB and C_{SUB} are used to generated the negative supply on pin C_{SUB} (about -2.5V), which can be used to power other external circuits, but it is low load current is noticeable.

R_{CAL1} and R_{CAL2} are used to set the drain current of FETs 1 & 3 and FETS 2 & 4. The R_{CAL} pins can also be used as logic inputs. If set to a logic high state (>3.0V), the associated FET bias stages are disabled, driving gate pins to -2.5V and switching drain pins open-circuit. This feature can be used as part of a power management system that turns off any unwanted stages in a multi input receiver. If any bias stages are not required, their gate and drain pins may be left open circuit. If all bias stages associated with an R_{CAL} resistor are not required, then this resistor may be omitted.

To protect the external FETs the circuits have been designed to ensure that, under any conditions including power up and powerdown transients, the gate drive from the bias circuits cannot exceed -3V. Additionally each stage has its own individual current limiter. Furthermore if the negative rail experiences a fault condition, such as overload or short circuit, the drain supply to the FETs will shut down avoiding excessive current flow.

■ TYPICAL CHARACTERISTICS