



7N60-HC

Power MOSFET

**7A, 600V N-CHANNEL
POWER MOSFET**

■ DESCRIPTION

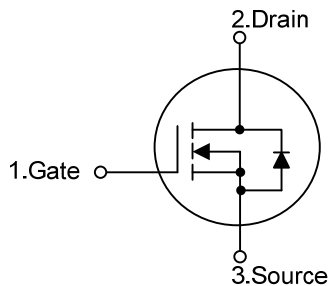
The UTC **7N60-HC** is a N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology allows a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **7N60-HC** is generally applied in high efficiency switch mode power supplies.

■ FEATURES

- * $R_{DS(ON)} < 1.1\Omega$ @ $V_{GS}=10V, I_D=3.5A$
- * Fast Switching
- * With 100% Avalanche Tested

■ SYMBOL

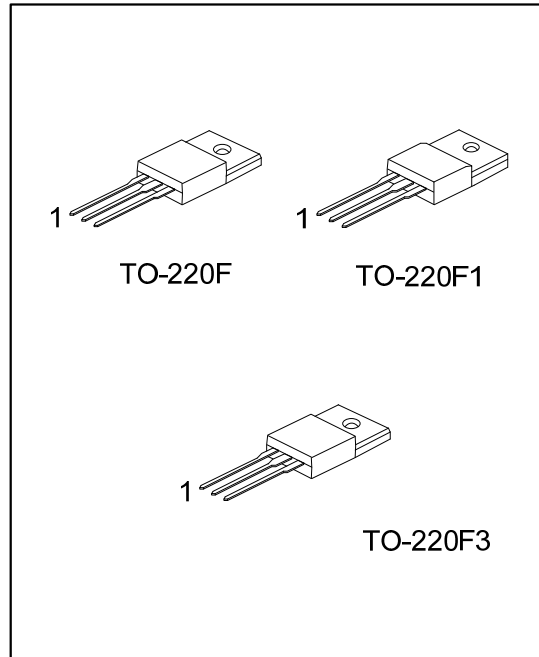


■ ORDERING INFORMATION

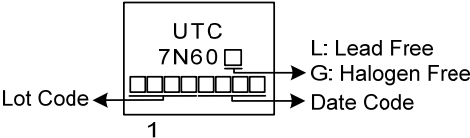
Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
7N60L-TF1-T	7N60G-TF1-T	TO-220F1	G	D	S	Tube
7N60L-TF3-T	7N60G-TF3-T	TO-220F	G	D	S	Tube
7N60L-TF3T-T	7N60G-TF3T-T	TO-220F3	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>7N60G-TF1-T</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) T: Tube (2) TF1: TO-220F1, TF3: TO-220F, TF3T: TO-220F3 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_c = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	600	V
Gate-Source Voltage	V_{GSS}	± 30	V
Drain Current	Continuous	I_D	7
	Pulsed (Note 2)	I_{DM}	14
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	555
Peak Diode Recovery dv/dt (Note 4)	dv/dt	2.5	V/ns
Power Dissipation	P_D	40	W
Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by maximum junction temperature.

3. $L=60\text{mH}$, $I_{AS}=4.3\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$

4. $I_{SD}\leq 7.0\text{A}$, $di/dt\leq 200\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	3.12	$^\circ\text{C}/\text{W}$

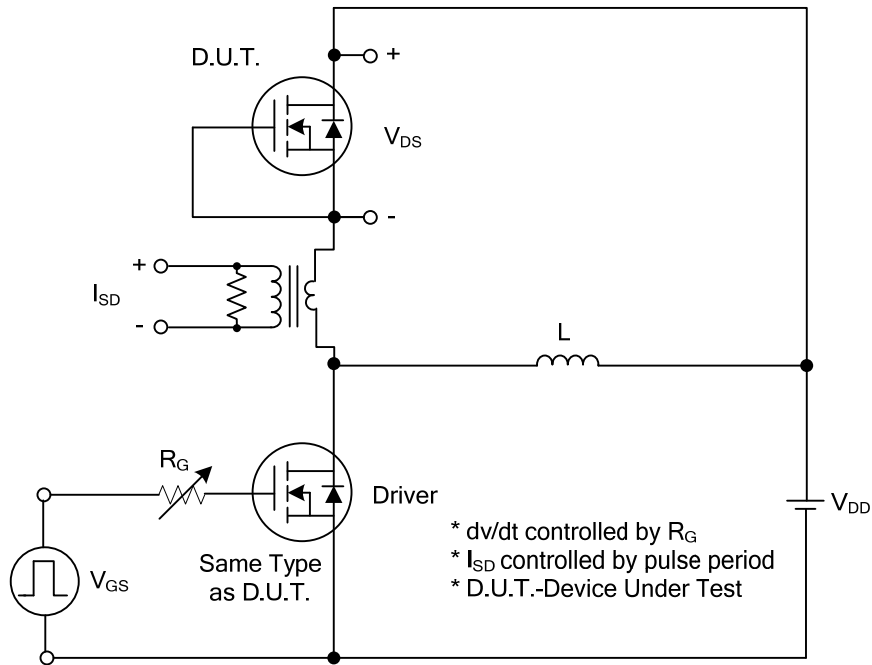
■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	600			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=600\text{V}$, $V_{GS}=0\text{V}$			10	μA
Gate-Source Leakage Current	Forward	I_{GSS}			100	nA
	Reverse				-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=3.5\text{A}$			1.1	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		860		pF
Output Capacitance	C_{OSS}			146		pF
Reverse Transfer Capacitance	C_{RSS}			36		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q_G	$V_{DS}=300\text{V}$, $V_{GS}=10\text{V}$, $I_D=7\text{A}$, $I_G=1\text{mA}$ (Note 1, 2)		35		nC
Gate to Source Charge	Q_{GS}			7.4		nC
Gate to Drain Charge	Q_{GD}			12.6		nC
Turn-ON Delay Time (Note 1)	$t_{D(ON)}$	$V_{DD}=30\text{V}$, $V_{GS}=10\text{V}$, $I_D=0.5\text{A}$, $R_G=25\Omega$ (Note 1, 2)		44		ns
Rise Time	t_R			106		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			278		ns
Fall-Time	t_F			180		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				7	A
Maximum Body-Diode Pulsed Current	I_{SM}				14	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S=7.0\text{A}$, $V_{GS}=0\text{V}$			1.4	V
Body Diode Reverse Recovery Time (Note 1)	t_{rr}	$I_S=7.0\text{A}$, $V_{GS}=0\text{V}$,		386		ns
Body Diode Reverse Recovery Charge	Q_{rr}	$di_F/dt=100\text{A}/\mu\text{s}$		3.4		μC

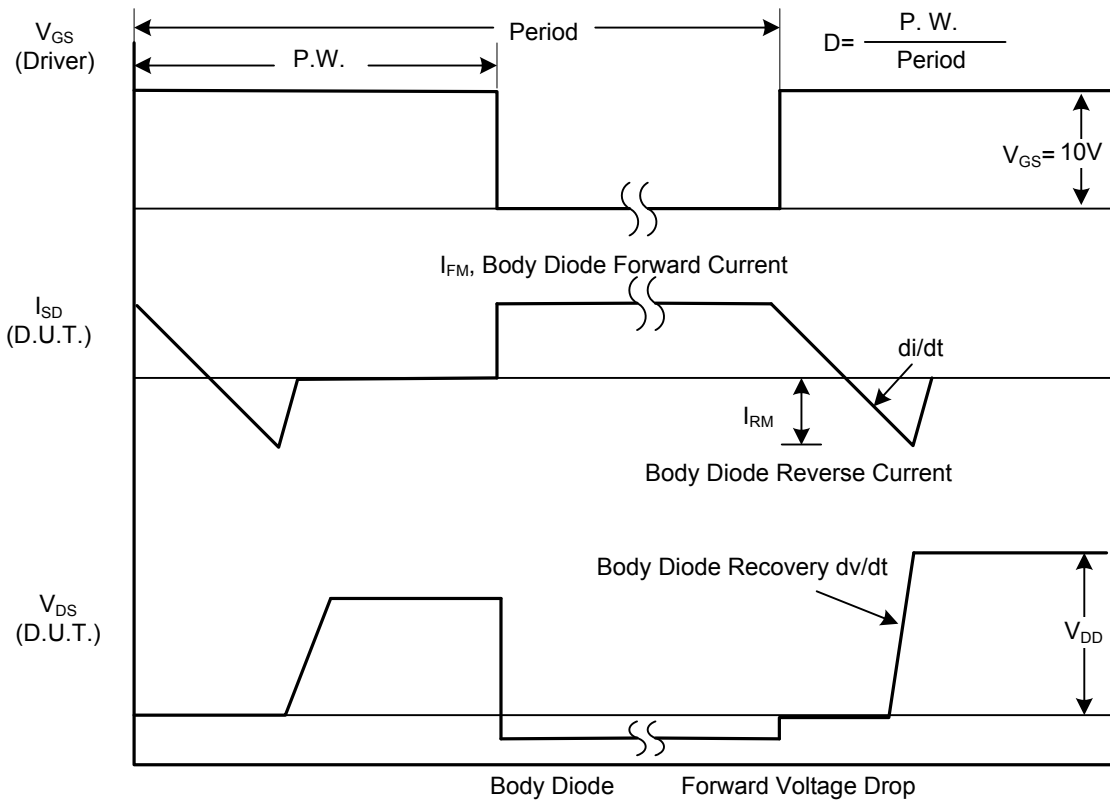
Notes: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

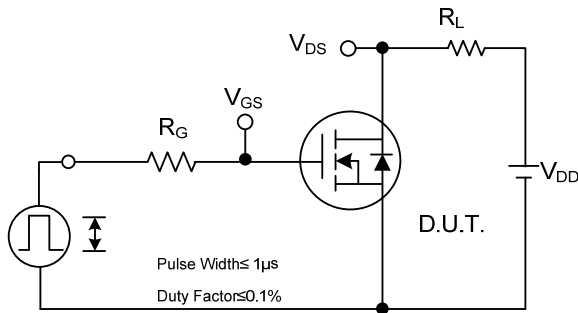


Peak Diode Recovery dv/dt Test Circuit

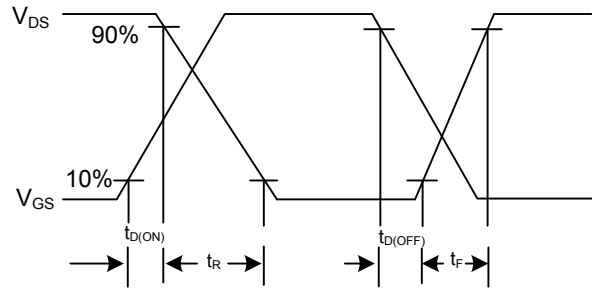


Peak Diode Recovery dv/dt Waveforms

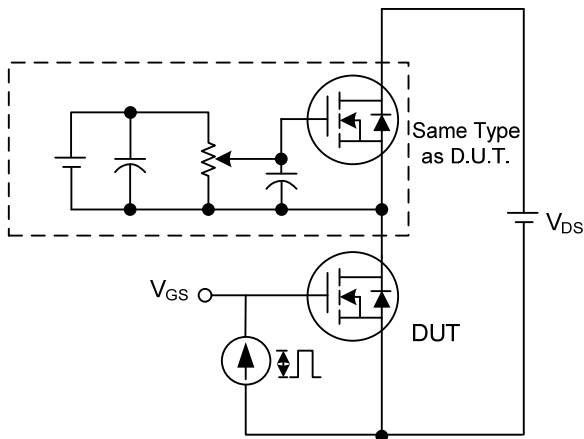
TEST CIRCUITS AND WAVEFORMS



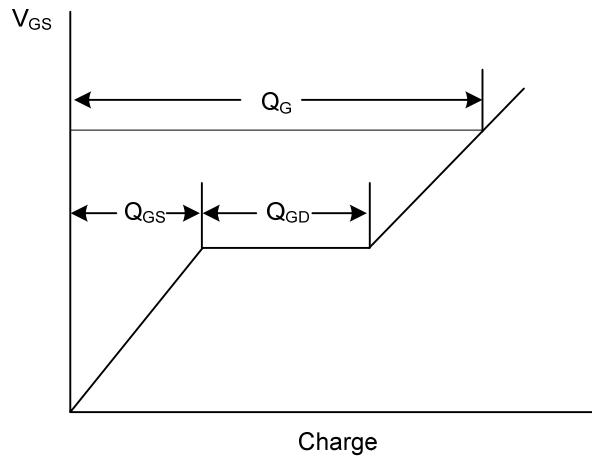
Switching Test Circuit



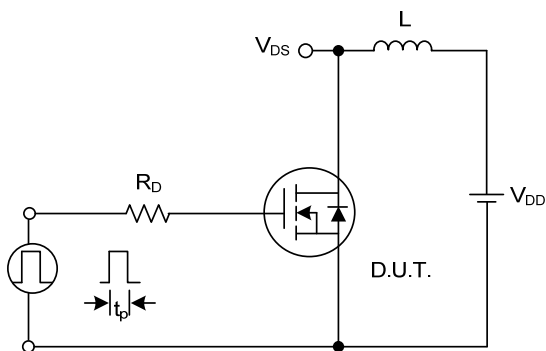
Switching Waveforms



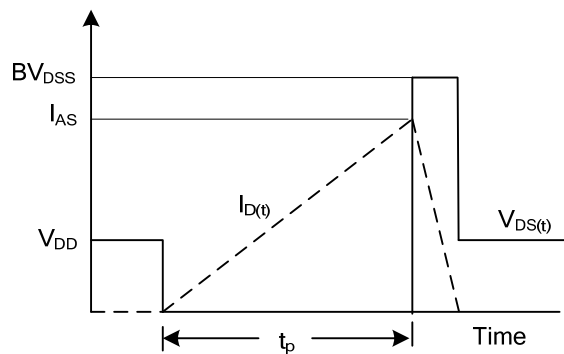
Gate Charge Test Circuit



Gate Charge Waveform

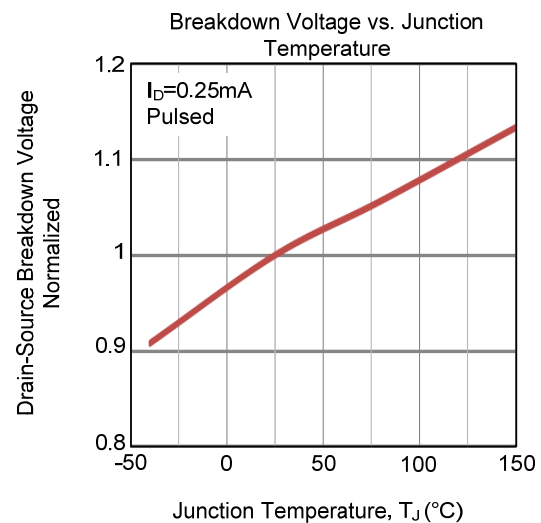
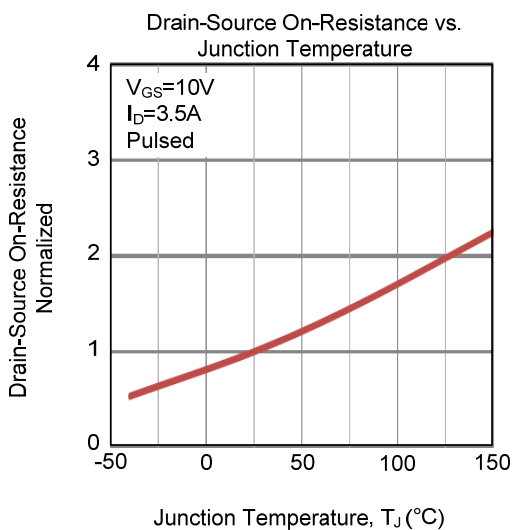
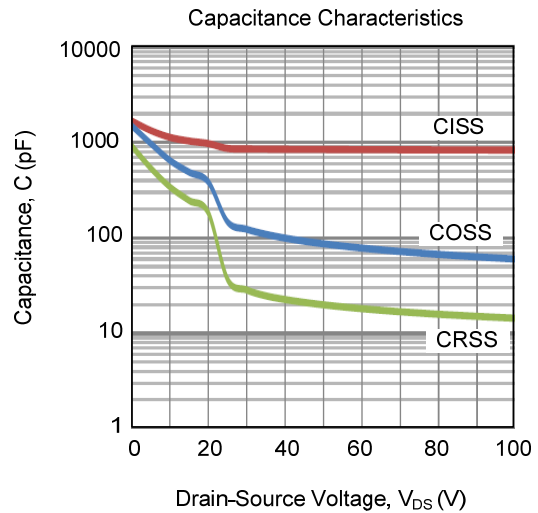
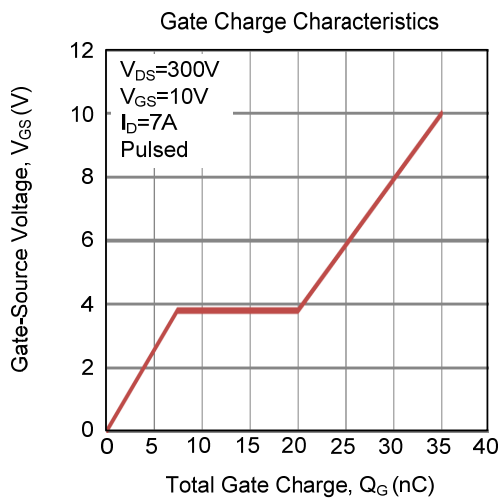
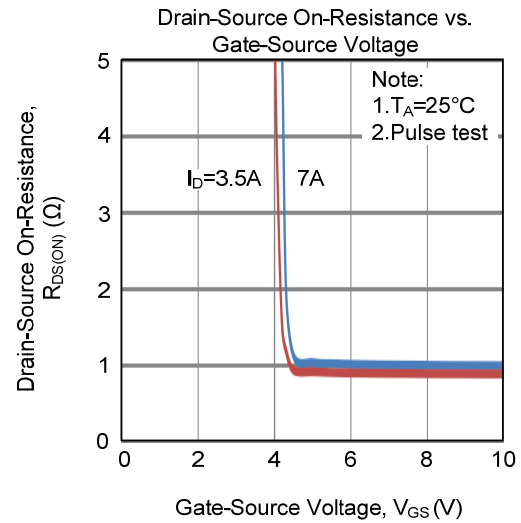
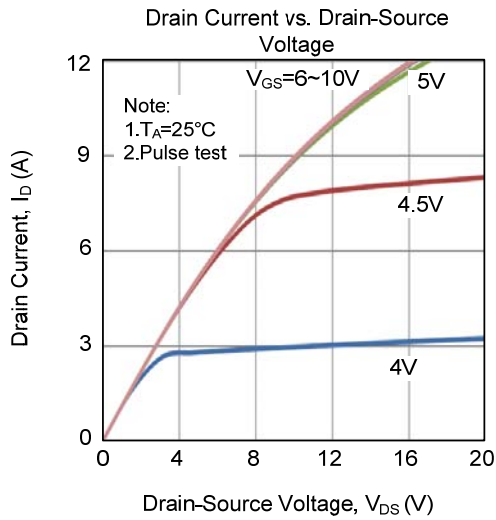


Unclamped Inductive Switching Test Circuit

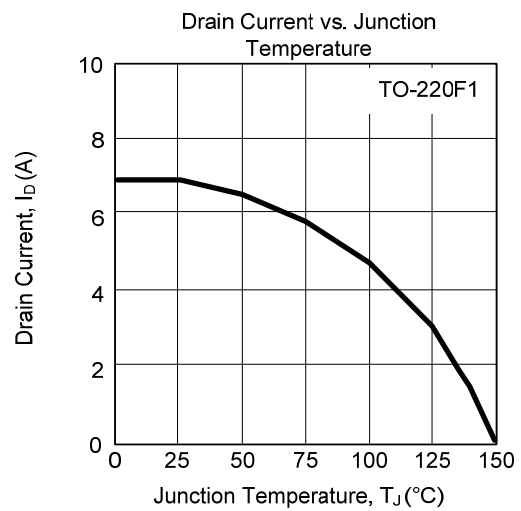
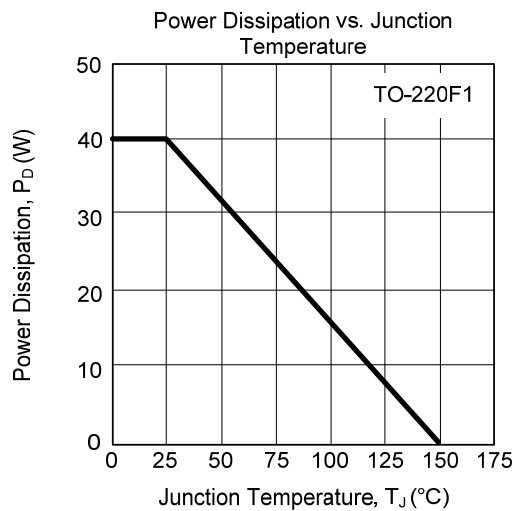
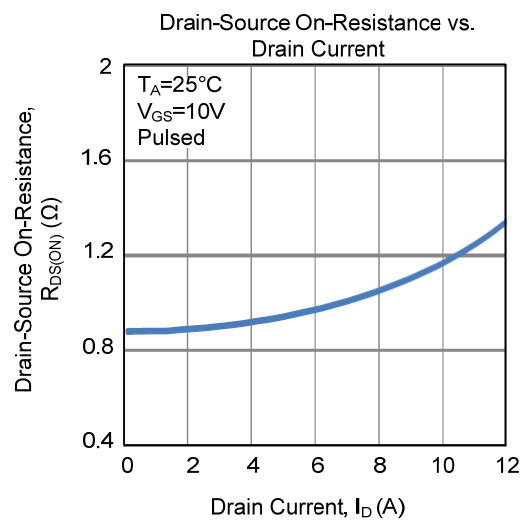
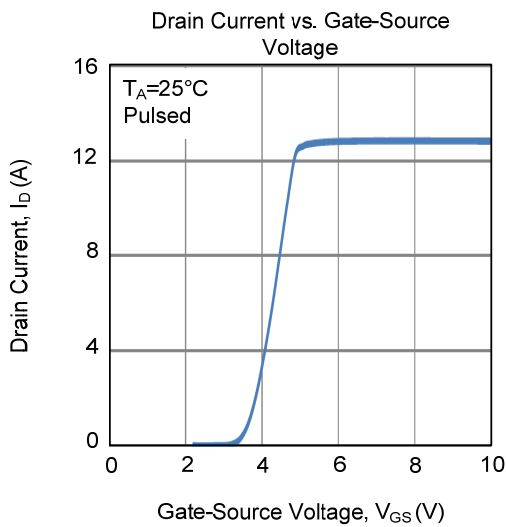
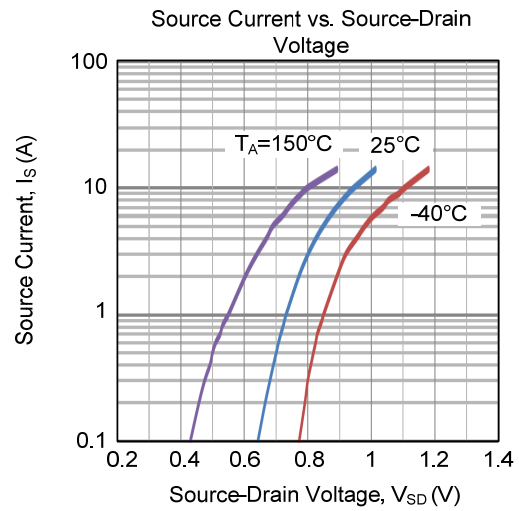
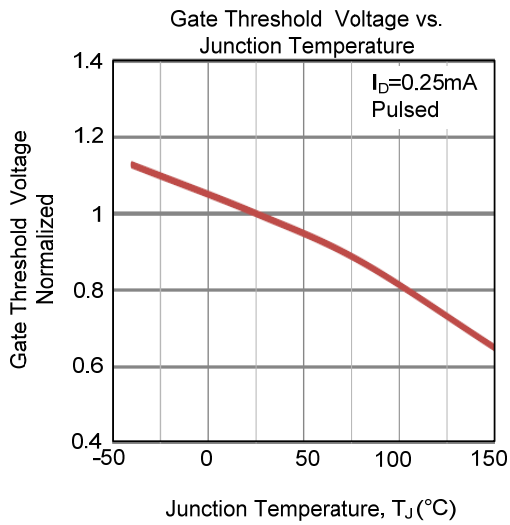


Unclamped Inductive Switching Waveforms

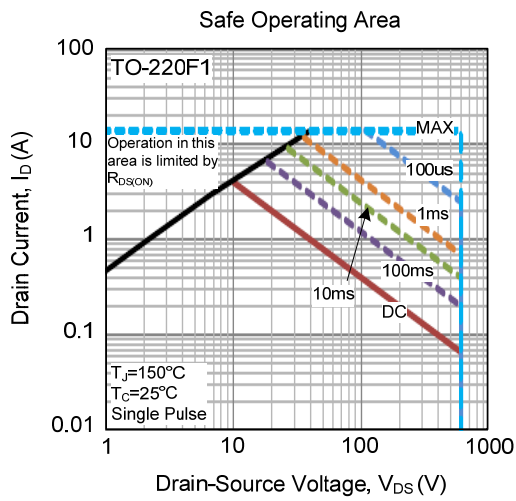
TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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