



## 6N50K-MT

Power MOSFET

### 6A, 500V N-CHANNEL POWER MOSFET

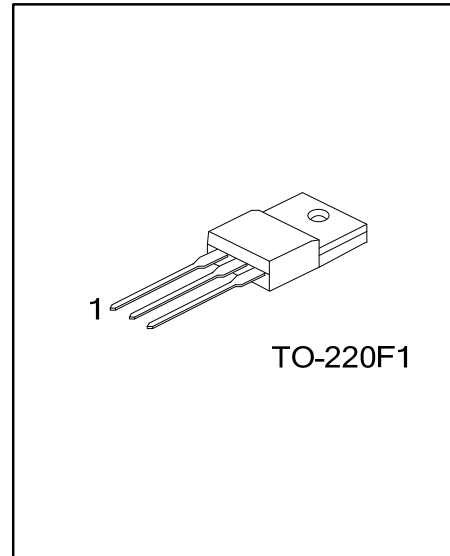
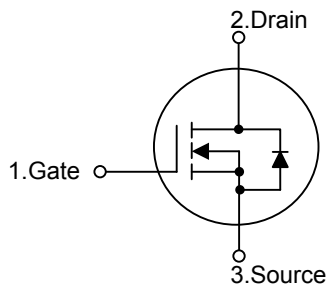
#### DESCRIPTION

The UTC **6N50K-MT** is a N-channel power MOSFET using UTC's advanced technology to provide the customers with minimum on-state resistance, superior switching performance and withstand high energy pulse in the avalanche and commutation mode.

#### FEATURES

- \*  $R_{DS(ON)} < 1.2\Omega$  @  $V_{GS}=10V, I_D=3.0A$
- \* High Switching Speed

#### SYMBOL



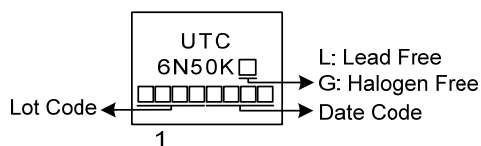
#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
6N50KL-TF1-T	6N50KG-TF1-T	TO-220F1	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>6N50KG-TF1-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) T: Tube</p> <p>(2) TF1: TO-220F1</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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#### MARKING



■ ABSOLUTE MAXIMUM RATINGS ( $T_C=25^\circ\text{C}$ , unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{DSS}$	500	V
Gate-Source Voltage		$V_{GSS}$	$\pm 30$	V
Drain Current	Continuous	$I_D$	6	A
	Pulsed (Note 2)	$I_{DM}$	12	A
Avalanche Energy	Single Pulsed (Note 3)	$E_{AS}$	328	mJ
Peak Diode Recovery dv/dt		dv/dt	3.5	V/ns
Power Dissipation		$P_D$	31	W
Junction Temperature		$T_J$	+150	$^\circ\text{C}$
Storage Temperature		$T_{STG}$	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3.  $L = 48 \text{ mH}$ ,  $I_{AS} = 3.7 \text{ A}$ ,  $V_{DD} = 50 \text{ V}$ ,  $R_G = 25 \Omega$ , Starting  $T_J = 25^\circ\text{C}$

4.  $I_{SD} \leq 6.0 \text{ A}$ ,  $di/dt \leq 200 \text{ A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	$\theta_{JA}$	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	$\theta_{JC}$	4	$^\circ\text{C}/\text{W}$

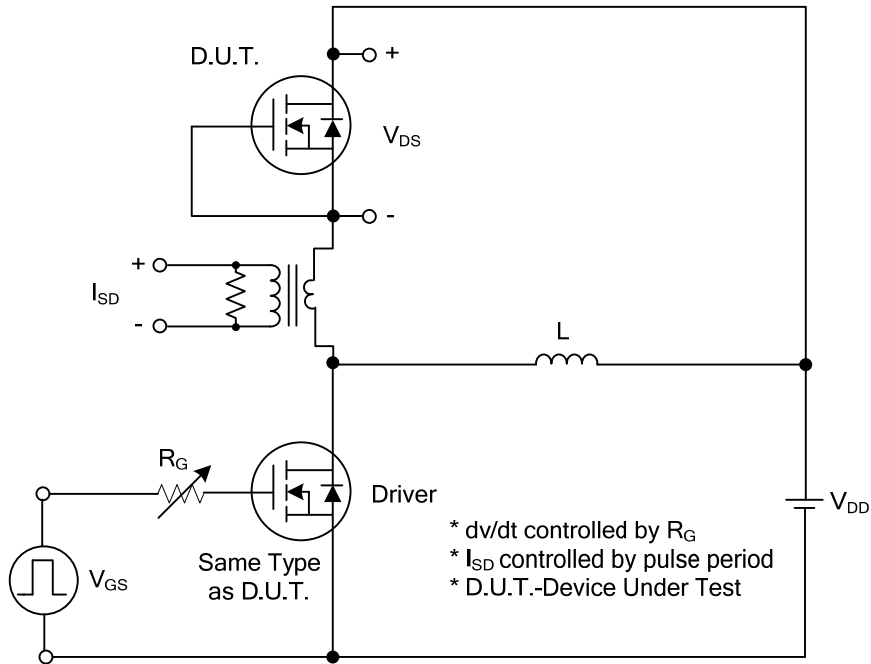
■ ELECTRICAL CHARACTERISTICS ( $T_C=25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$I_D=250\mu\text{A}$ , $V_{GS}=0\text{V}$	500			V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=500\text{V}$ , $V_{GS}=0\text{V}$			10	$\mu\text{A}$
Gate- Source Leakage Current	$I_{GSS}$	Forward			+100	nA
		Reverse			-100	nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$ , $I_D=3.0\text{A}$			1.2	$\Omega$
<b>DYNAMIC PARAMETERS</b>						
Input Capacitance	$C_{ISS}$	$V_{GS}=0\text{V}$ , $V_{DS}=25\text{V}$ , $f=1.0\text{MHz}$		700		pF
Output Capacitance	$C_{OSS}$			90		pF
Reverse Transfer Capacitance	$C_{RSS}$			8		pF
<b>SWITCHING PARAMETERS</b>						
Total Gate Charge (Note 1)	$Q_G$	$V_{DS}=200\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=6.0\text{A}$ $I_G=1\text{mA}$ (Note1, 2)		19		nC
Gate to Source Charge	$Q_{GS}$			4		nC
Gate to Drain Charge	$Q_{GD}$			4.3		nC
Turn-ON Delay Time (Note 1)	$t_{D(ON)}$	$V_{DS}=250\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=6.0\text{A}$ , $R_G=25\Omega$ (Note1, 2)		2.6		ns
Rise Time	$t_R$			10		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			36		ns
Fall-Time	$t_F$			14.2		ns
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Maximum Body-Diode Continuous Current	$I_S$				6	A
Maximum Body-Diode Pulsed Current	$I_{SM}$				12	A
Drain-Source Diode Forward Voltage (Note 1)	$V_{SD}$	$I_S=6.0\text{A}$ , $V_{GS}=0\text{V}$			1.4	V
Body Diode Reverse Recovery Time (Note 1)	$t_{rr}$	$I_S=6.0\text{A}$ , $V_{GS}=0\text{V}$ , $dI_F/dt=100\text{A}/\mu\text{s}$ (Note 1)		260		ns
Reverse Recovery Charge	$Q_{rr}$			2.2		$\mu\text{C}$

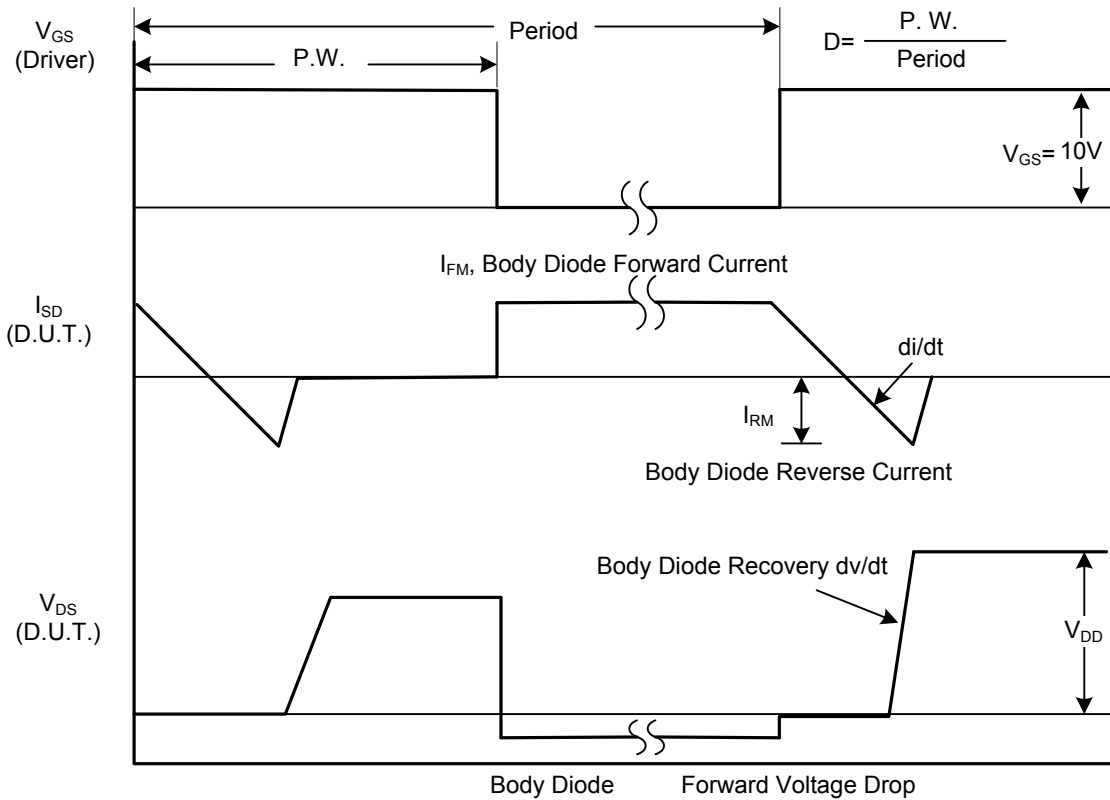
Notes: 1. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$ .

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

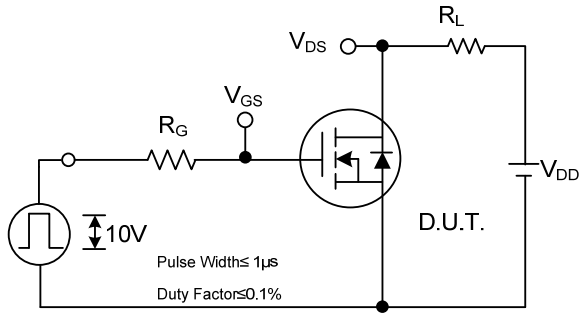


Peak Diode Recovery dv/dt Test Circuit

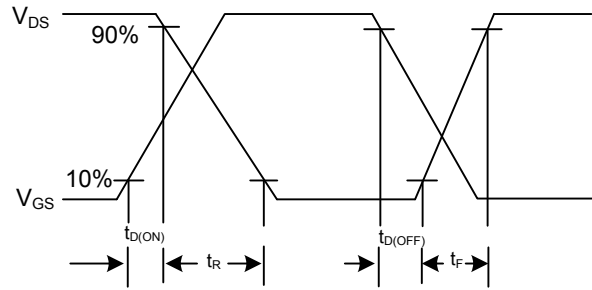


Peak Diode Recovery dv/dt Waveforms

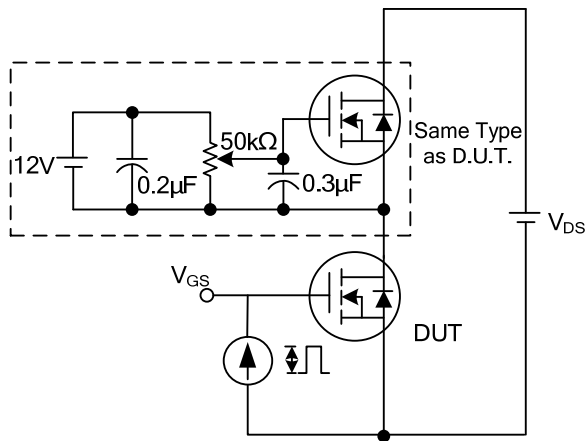
## TEST CIRCUITS AND WAVEFORMS (Cont.)



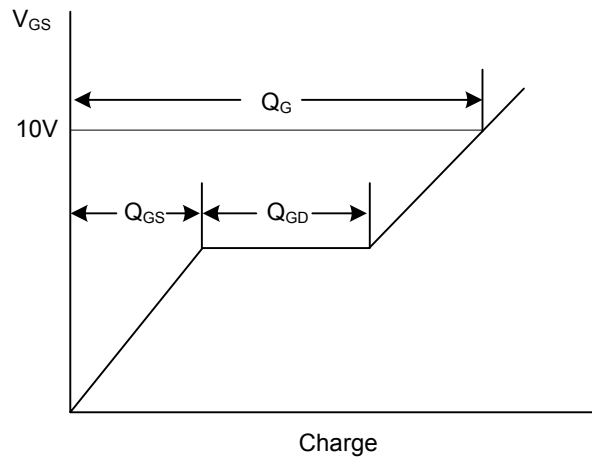
Switching Test Circuit



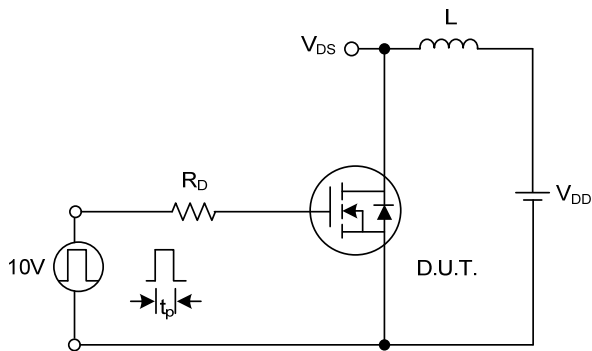
Switching Waveforms



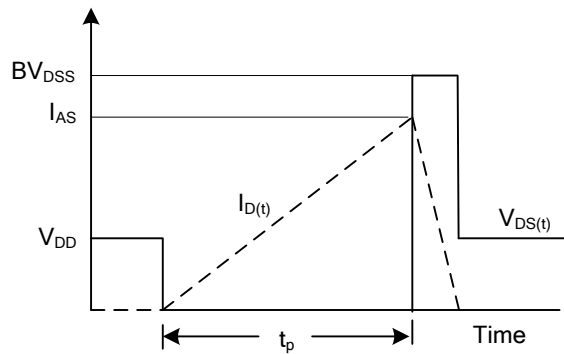
Gate Charge Test Circuit



Gate Charge Waveform

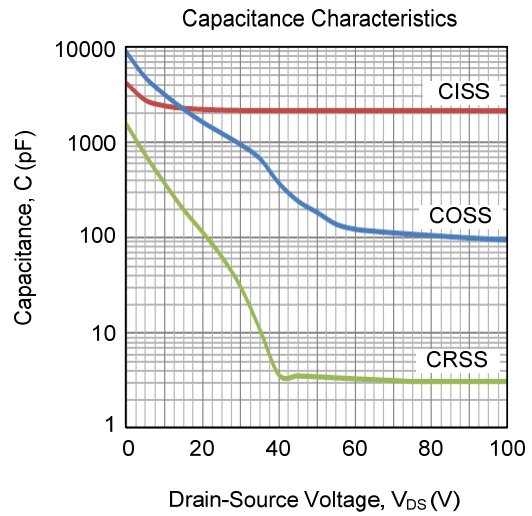
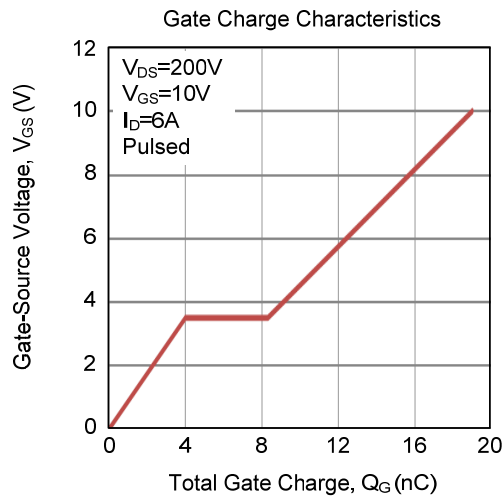


Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

### TYPICAL CHARACTERISTICS



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