



8N50-MT

Power MOSFET

8A, 500V N-CHANNEL POWER MOSFET

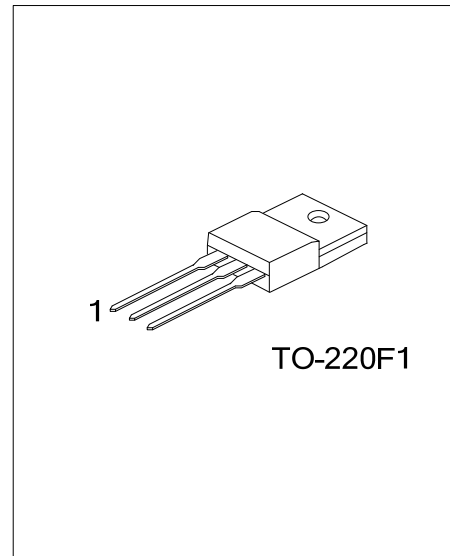
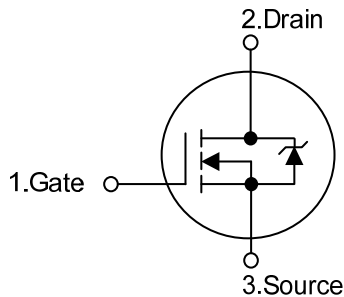
DESCRIPTION

The N-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications such as switching regulators, switching converters, solenoid, motor drivers, relay drivers.

FEATURES

- * Low $R_{DS(ON)} < 0.87\Omega @ V_{GS}=10V, I_D = 4.4A$
- * Single Pulse Avalanche Energy Rated
- * Fast Switching Speeds
- * Linear Transfer Characteristics
- * High Input Impedance

SYMBOL



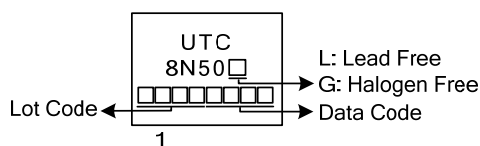
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen-Free		1	2	3	
8N50L-TF1-T	8N50G-TF1-T	TO-220F1	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>8N50G-TF1-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) T: Tube</p> <p>(2) TF1: TO-220F1</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless Otherwise Specified)

PARAMETER	SYMBOL	RATINGS	UNIT	
Drain to Source Voltage ($T_J = 25^\circ\text{C} \sim 125^\circ\text{C}$)	V_{DSS}	500	V	
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$, $T_J = 25^\circ\text{C} \sim 125^\circ\text{C}$)	V_{DGR}	500	V	
Gate to Source Voltage	V_{GSS}	± 30	V	
Drain Current (Note 2)	Continuous	I_D	8.0	A
	Pulsed	I_{DM}	32	A
Single Pulse Avalanche Energy (Note 3)	E_{AS}	336	mJ	
Peak Diode Recovery dv/dt (Note 4)	dv/dt	3.3	V/ns	
Power Dissipation	P_D	44	W	
Junction Temperature	T_J	+150	$^\circ\text{C}$	
Storage Temperature	T_{STG}	-55 ~ +150	$^\circ\text{C}$	

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 10\text{mH}$, $I_{AS} = 8.0\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.

4. $I_{SD} \leq 8.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$.

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	2.7	$^\circ\text{C}/\text{W}$

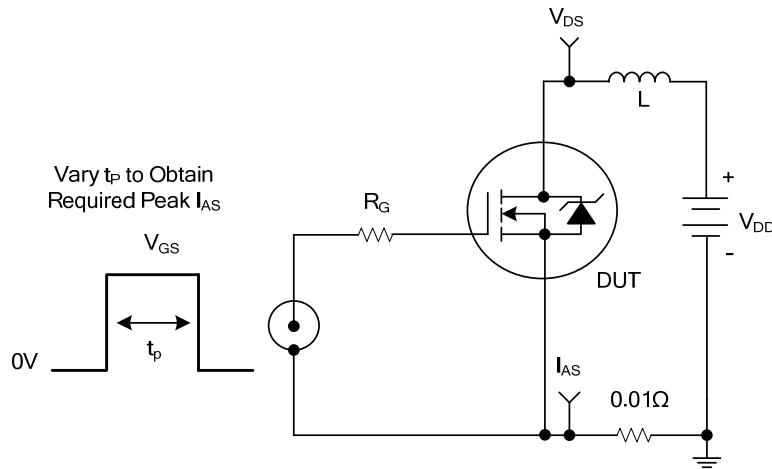
■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	500			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}$, $V_{GS} = 0\text{V}$			25	μA
Gate-Source Leakage Current	Forward	I_{GSS}			+100	nA
					Reverse	-100
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{V}$, $I_D = 4.4\text{A}$			0.87	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{MHz}$		920		pF
Output Capacitance	C_{OSS}			105		pF
Reverse Transfer Capacitance	C_{RSS}			10		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q_G	$V_{DS} = 400\text{V}$, $V_{GS} = 10\text{V}$, $I_D = 8\text{A}$, $I_G = 10\text{mA}$ (Note 1, 2)		24		nC
Gate to Source Charge	Q_{GS}			3		nC
Gate to Drain Charge	Q_{GD}			2		nC
Turn-on Delay Time (Note 1)	$t_{D(ON)}$	$V_{DS} = 250\text{V}$, $V_{GS} = 10\text{V}$, $I_D = 8\text{A}$, $R_G = 25\Omega$ (Note 1, 2)		4.8		ns
Rise Time	t_R			11.6		ns
Turn-off Delay Time	$t_{D(OFF)}$			56		ns
Fall-Time	t_F			20		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				8	A
Maximum Body-Diode Pulsed Current	I_{SM}				32	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S = 8.0\text{A}$, $V_{GS} = 0\text{V}$			2	V
Reverse Recovery Time (Note 1)	t_{rr}	$I_S = 8.0\text{A}$, $V_{GS} = 0\text{V}$, $dI_F/dt = 100\text{A}/\mu\text{s}$		312		nS
Reverse Recovery Charge	Q_{rr}			3.1		μC

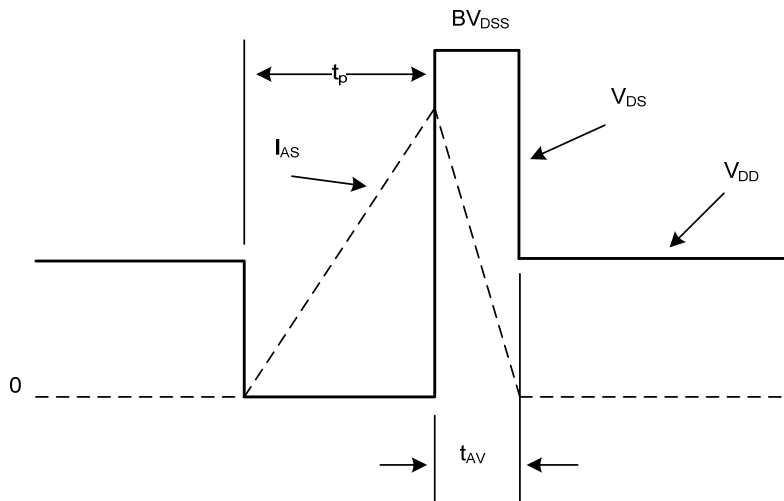
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

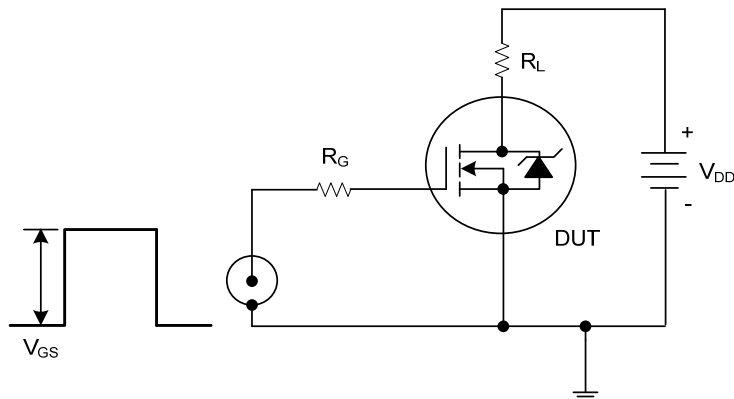
■ TEST CIRCUITS AND WAVEFORMS



Unclamped Energy Test Circuit

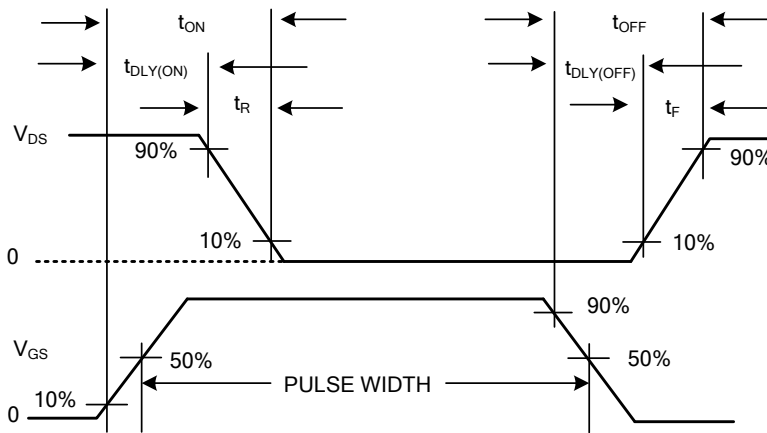


Unclamped Energy Waveforms

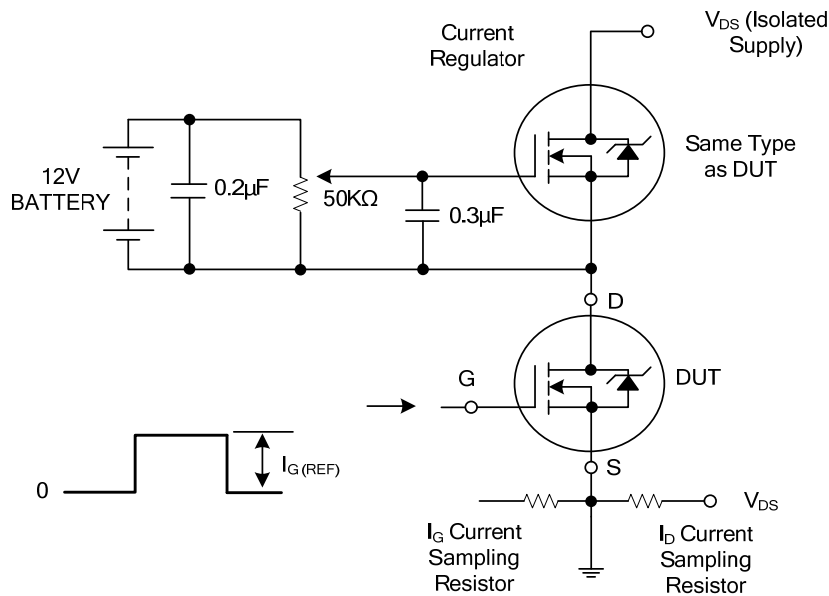


Switching Time Test Circuit

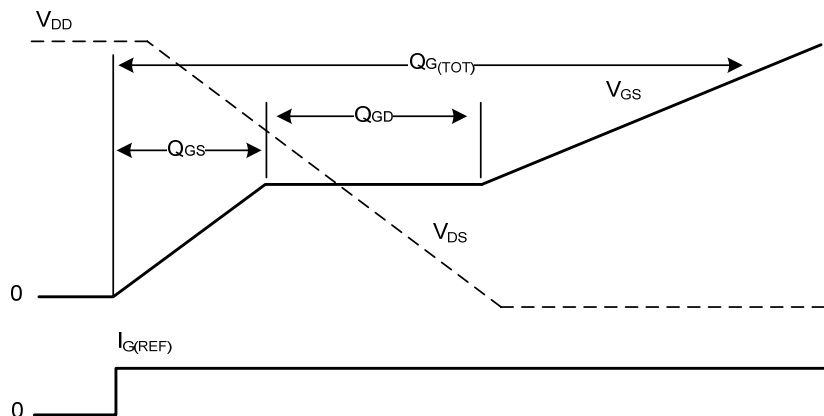
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



Resistive Switching Waveforms

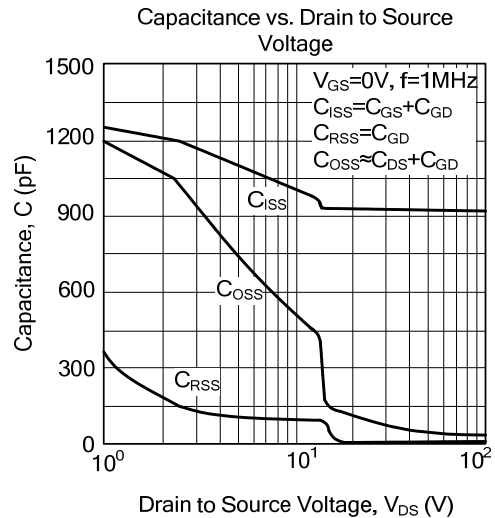
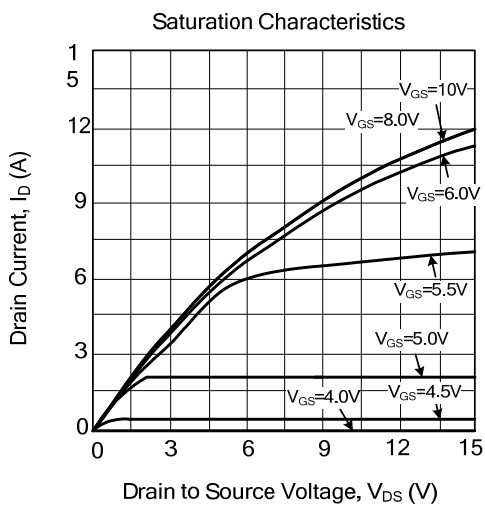
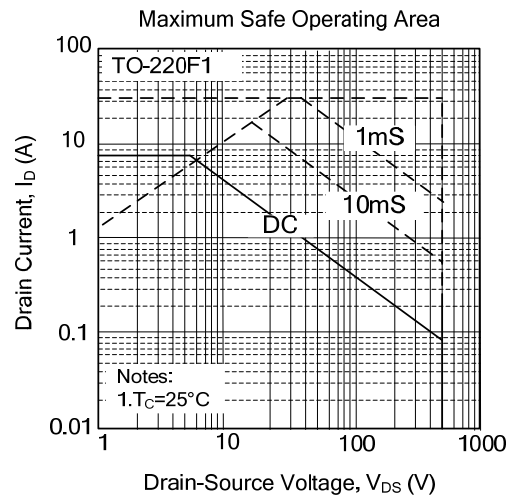
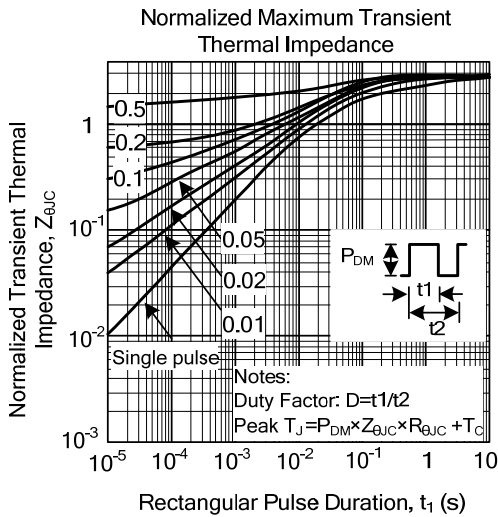
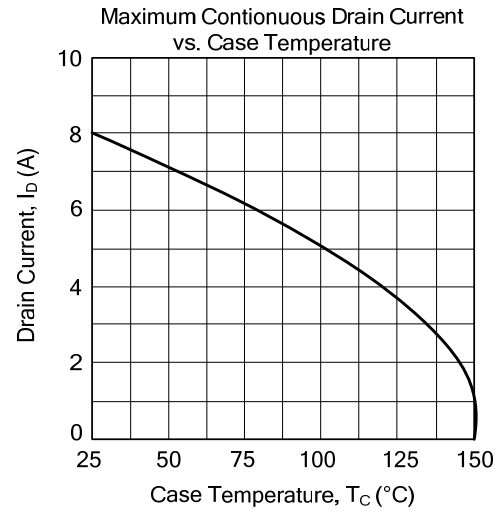
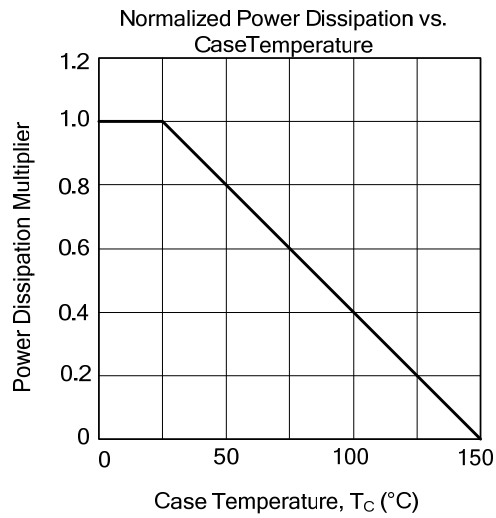


Gate Charge Test Circuit

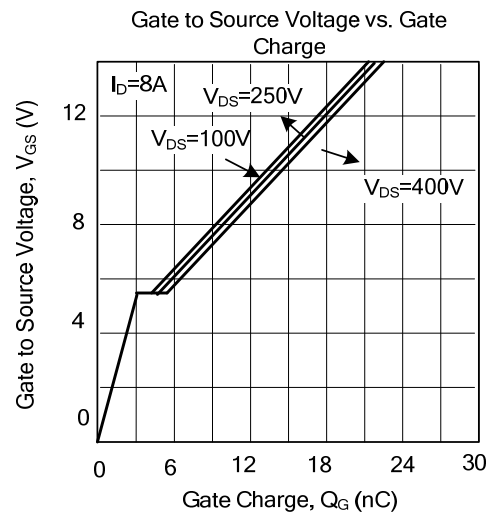
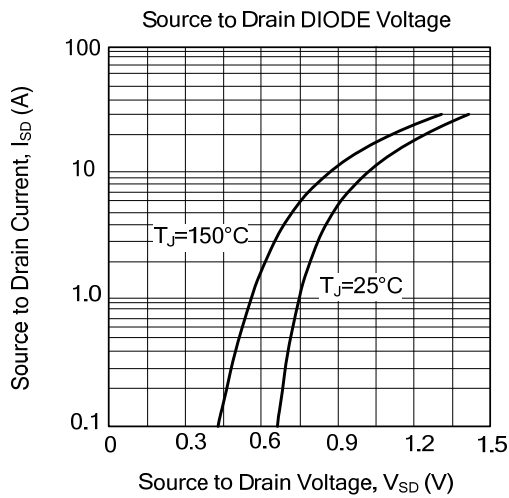
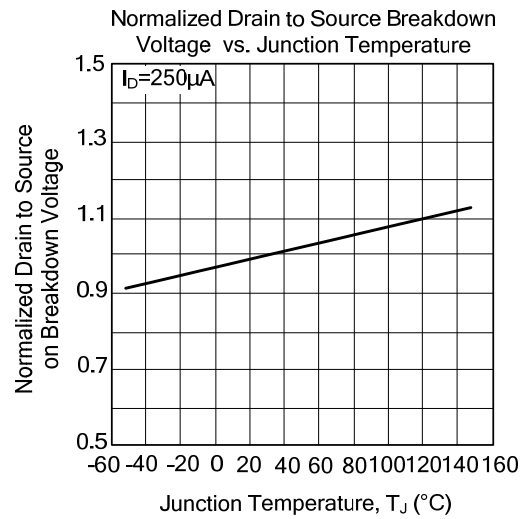
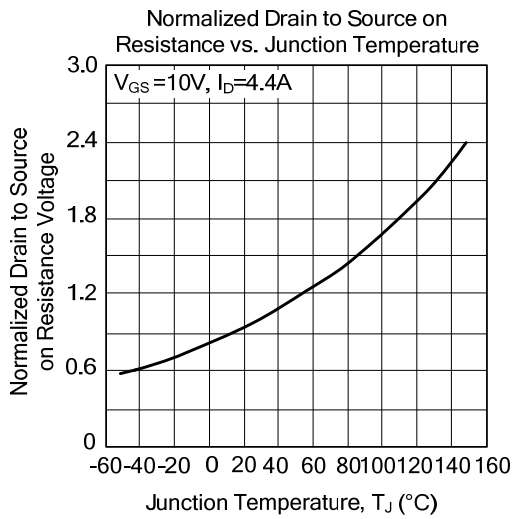
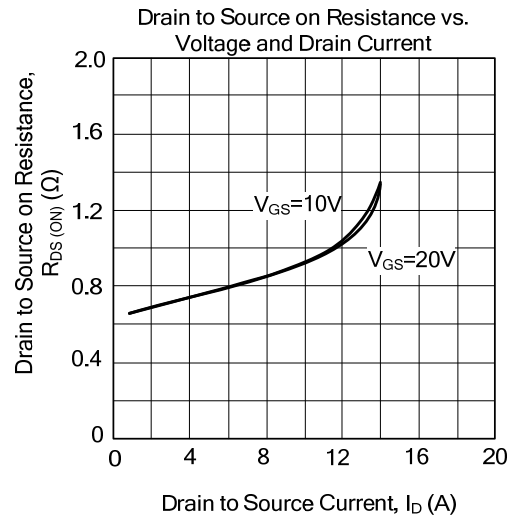
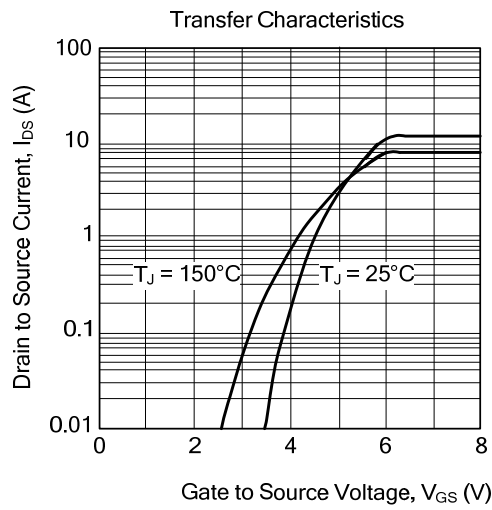


Gate Charge Waveforms

TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



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