



## ULN2012

Preliminary

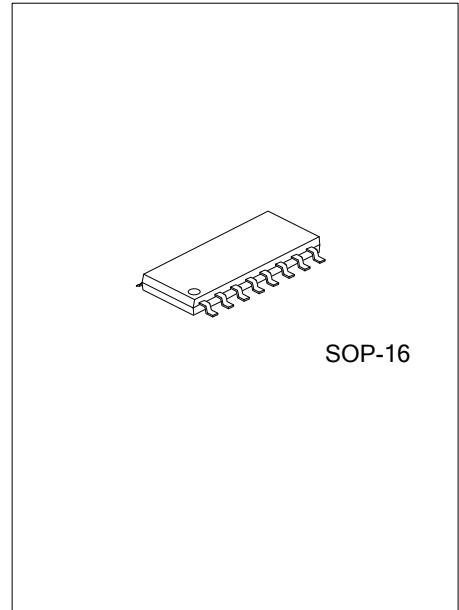
LINEAR INTEGRATED CIRCUIT

### HIGH VOLTAGE HIGH CURRENT DARLINGTON ARRAY

#### DESCRIPTION

The UTC **ULN2012** is high-voltage, high-current Darlington transistor arrays. Each consists of seven NPN Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 600mA. All units feature integral clamp diodes for switching inductive loads. Applications include relay, hammer, lamp and display (LED) drivers.

The UTC **ULN2012** is intended for use with 14 to 25V PMOS logic. Each input has a series Zener diode and current limiting resistor. The Zener diode also provides excellent noise immunity for this device.



SOP-16

#### FEATURES

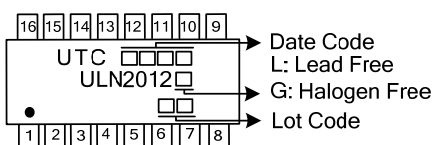
- \* PMOS Compatible Inputs
- \* Output Current to 600mA
- \* Output Voltage to 50V
- \* Transient-Protected Outputs

#### ORDERING INFORMATION

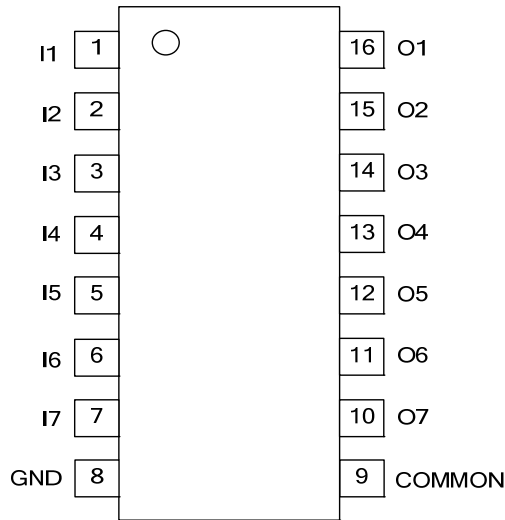
Ordering Number		Package	Packing
Lead Free	Halogen Free		
ULN2012L-S16-R	ULN2012G-S16-R	SOP-16	Tape Reel

<p>ULN2012G-S16-R</p> <ul style="list-style-type: none"> <li>(1) Packing Type</li> <li>(2) Package Type</li> <li>(3) Green Package</li> </ul>	<ul style="list-style-type: none"> <li>(1) R: Tape Reel</li> <li>(2) S16: SOP-16</li> <li>(3) G: Halogen Free and Lead Free, L: Lead Free</li> </ul>
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#### MARKING



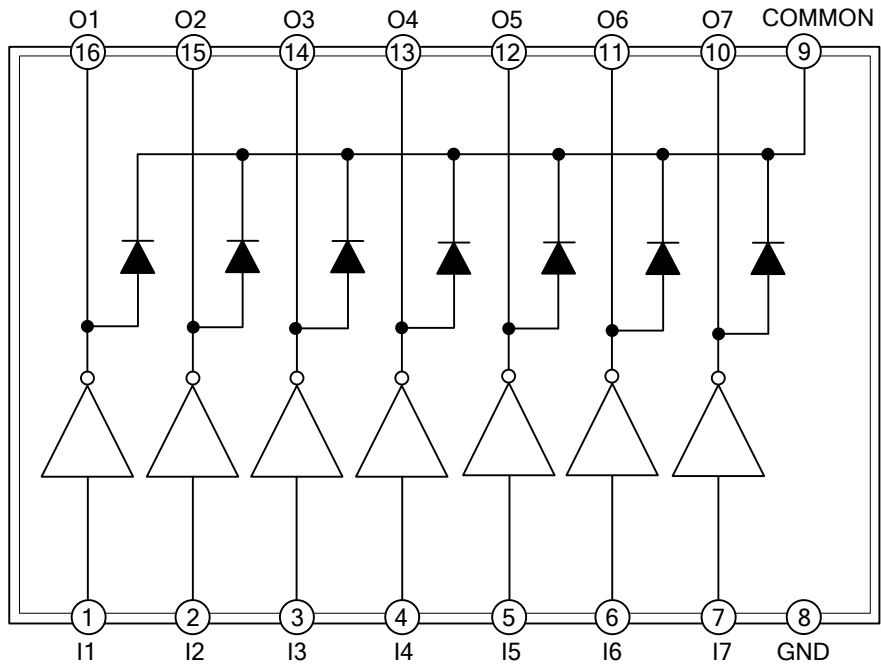
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	I1	1 Channel Input Pin
2	I2	2 Channel Input Pin
3	I3	3 Channel Input Pin
4	I4	4 Channel Input Pin
5	I5	5 Channel Input Pin
6	I6	6 Channel Input Pin
7	I7	7 Channel Input Pin
8	GND	Ground
9	COMMON	Clamp Diode
10	O7	7 Channel Output Pin
11	O6	6 Channel Output Pin
12	O5	5 Channel Output Pin
13	O4	4 Channel Output Pin
14	O3	3 Channel Output Pin
15	O2	2 Channel Output Pin
16	O1	1 Channel Output Pin

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Output Sustaining Voltage	$V_{OUT}$	-0.5 ~ 50	V
Input Voltage	$V_{IN}$	-0.5 ~ 30	V
Clamp Diode Reverse Voltage	$V_R$	50	V
Output Current	$I_{OUT}$	600	mA /ch
Clamp Diode Forward Current	$I_F$	600	mA
Power Dissipation	$P_D$	1.25 (Note 2)	W
Junction Temperature	$T_J$	+125	°C
Operating Temperature	$T_{OPR}$	-40 ~ +85	°C
Storage Temperature	$T_{STG}$	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. On PCB (Test Board: JEDEC 2s2p)

■ ELECTRICAL CHARACTERISTICS ( $T_A=25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CIRCUIT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Leakage Current	$I_{CEX}$	1	$V_{CE} = 50\text{V}$ , $V_{IN} = 6.0\text{V}$			50	$\mu\text{A}$
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	$I_{OUT} = 200\text{mA}$ , $I_{IN} = 350\mu\text{A}$		1.1	1.3	V
			$I_{OUT} = 350\text{mA}$ , $I_{IN} = 500\mu\text{A}$		1.3	1.6	V
			$I_{OUT} = 500\text{mA}$ , $I_{IN} = 600\mu\text{A}$		1.7	1.9	V
Input Current (Output On)	$I_{IN(ON)}$	3	$V_{IN} = 17\text{V}$		0.82	1.25	mA
Input Current (Output Off)	$I_{IN(OFF)}$	4	$I_C = 500\mu\text{A}$	50	65		$\mu\text{A}$
Input Voltage (Output On)	$V_{IN(ON)}$	5	$V_{CE} = 2\text{V}$ , $I_C = 500\text{mA}$			17	V
Clamp Diode Reverse Current	$I_R$	6	$V_R = 50\text{V}$ , $T_A = 25^\circ\text{C}$			50	$\mu\text{A}$
			$V_R = 50\text{V}$ , $T_A = 85^\circ\text{C}$			100	$\mu\text{A}$
Clamp Diode Forward Voltage	$V_F$	7	$I_F = 350\text{mA}$		1.7	2.0	V
			$I_F = 500\text{mA}$		2.1	2.5	V
Input Capacitance	$C_{IN}$				15	25	pF
Turn-On Delay	$t_{ON}$	8	$0.5E_{in}$ to $0.5E_{out}$		0.45		$\mu\text{s}$
Turn-Off Delay	$t_{OFF}$	8	$0.5E_{in}$ to $0.5E_{out}$		0.2		$\mu\text{s}$

■ TEST CIRCUIT

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

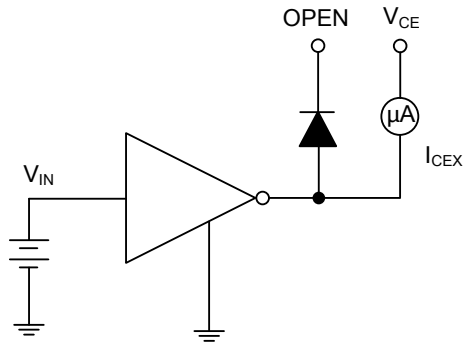


Figure 1

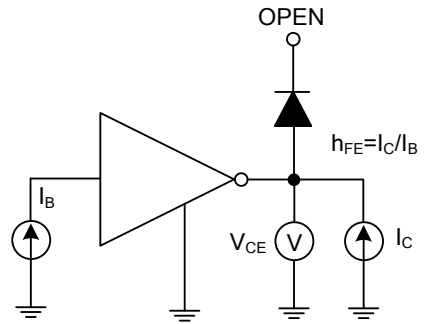


Figure 2

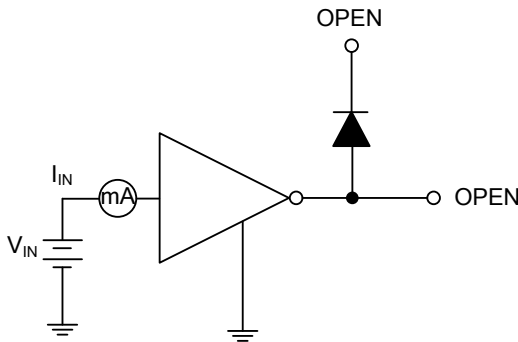


Figure 3

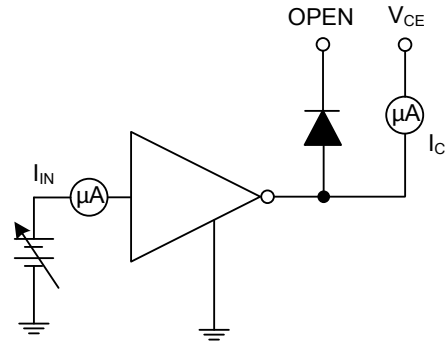


Figure 4

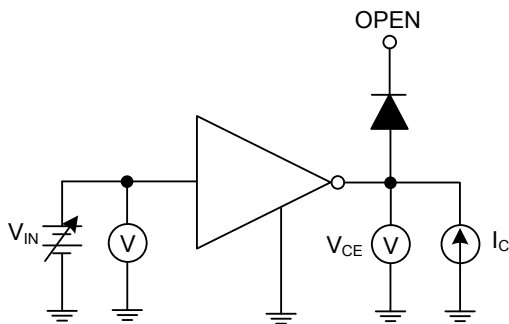


Figure 5

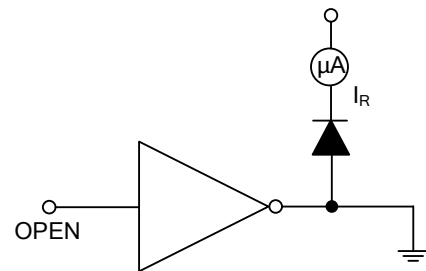


Figure 6

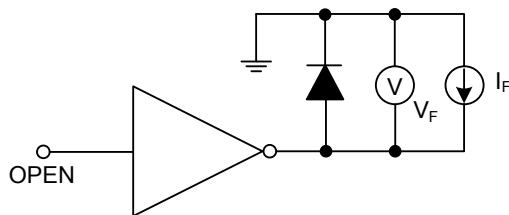


Figure 7

■ TEST CIRCUIT (Cont.)

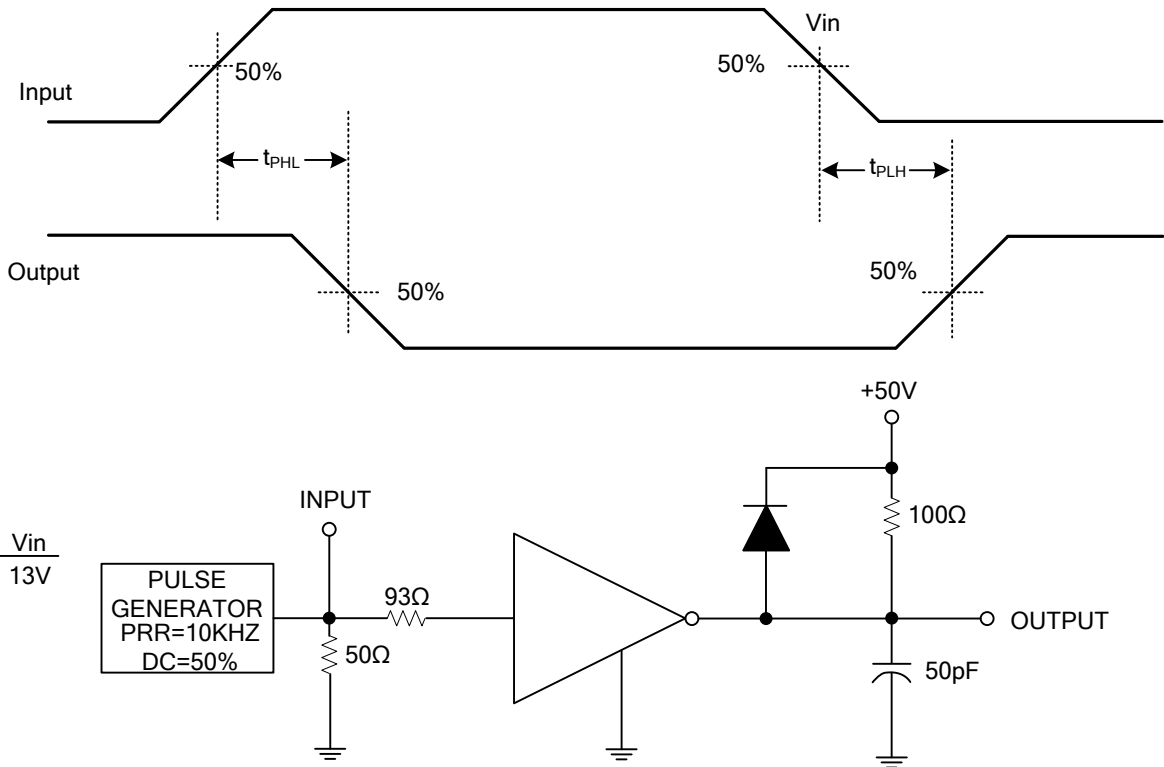
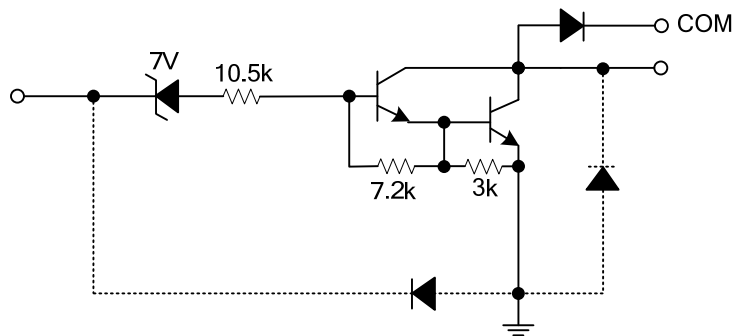


Figure 8

■ TYPICAL APPLICATION CIRCUIT



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