UTT100N07 Power MOSFET

# 100A, 65V N-CHANNEL POWER MOSFET

#### **■** DESCRIPTION

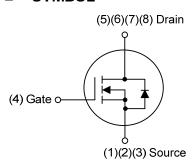
UTC **UTT100N07** is a N-Channel enhancement mode power field effect transistors are using trench DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.



- \*  $R_{DS(ON)} \le 2.8 \text{ m}\Omega$  @  $V_{GS}$ =10V,  $I_{D}$ =20A  $R_{DS(ON)} \le 5.4 \text{ m}\Omega$  @  $V_{GS}$ =4.5V,  $I_{D}$ =10A
- \* Improved dv/dt capability
- \* Fast switching
- \* 100% EAS Guaranteed

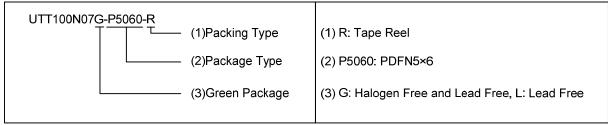
#### ■ SYMBOL

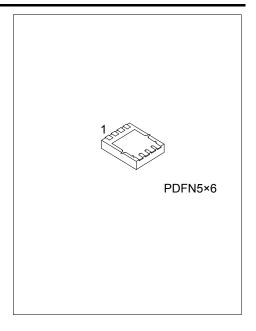


# **■ ORDERING INFORMATION**

Ordering Number		Doolsons	Pin Assignment								Da alaina	
Lead Free	Halogen Free	Package	1	2	3	4	5	6	7	8	Packing	
UTT100N07L-P5060-R	UTT100N07G-P5060-R	PDFN5×6	S	S	S	G	D	D	D	D	Tape Reel	

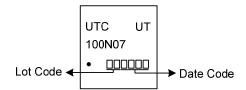
Note: Pin Assignment: G: Gate D: Drain S: Source





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# ■ MARKING



UTT100N07 Power MOSFET

# ■ ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT	
Drain-Source Voltage		$V_{DSS}$	65	V	
Gate-Source Voltage		$V_{GSS}$	+20 / -12	V	
Drain Current	Continuous	T <sub>C</sub> =25°C	I <sub>D</sub>	100	Α
		T <sub>C</sub> =100°C		63	Α
	Pulsed (Note 2)		$I_{DM}$	400	Α
Avalanche Energy (Note 3) Single Pulsed			E <sub>AS</sub>	245	mJ
Power Dissipation			$P_D$	142	W
Junction Temperature			$T_J$	+150	°C
Storage Temperature			$T_{STG}$	-55 ~ <b>+</b> 150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

- 2. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 3. L=0.1mH,  $I_{AS}$ =70A,  $V_{DD}$ =25V,  $R_{G}$ =25  $\Omega$ , Starting  $T_{J}$  = 25°C.
- 4.  $I_{SD} \le 3.0A$ , di/dt $\le 200A/\mu s$ ,  $V_{DD} \le BV_{DSS}$ , Starting  $T_J = 25$ °C.

#### ■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	$\theta_{JA}$	62	°C/W
Junction to Case	$\theta_{ m JC}$	0.88	°C/W

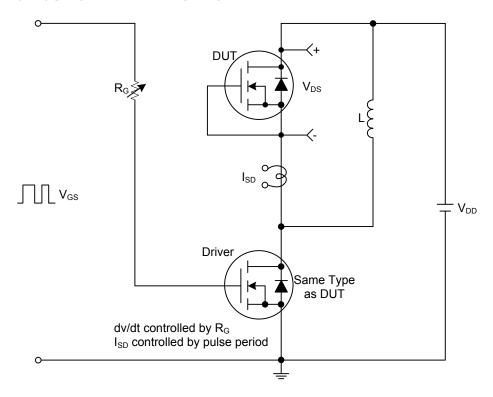
## ■ ELECTRICAL CHARACTERISTICS (T<sub>J</sub> =25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
OFF CHARACTERISTICS									
Drain-Source Breakdown Voltage		$BV_{DSS}$	$I_D = 250 \mu A, V_{GS} = 0 V$	65			V		
Drain-Source Leakage Current		I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V			1	μΑ		
			V <sub>DS</sub> =48V, V <sub>GS</sub> =0V			10	μΑ		
Cata Course Laglage Current	orward	I <sub>GSS</sub>	V <sub>GS</sub> =+20V, V <sub>DS</sub> =0V			+100	nA		
Gate-Source Leakage Current	Reverse		V <sub>GS</sub> =-20V, V <sub>DS</sub> =0V			-100	nA		
ON CHARACTERISTICS									
Gate Threshold Voltage		$V_{GS(TH)}$	$V_{DS}=V_{GS}$ , $I_{D}=250\mu A$	1.0	1.6	2.5	V		
Static Drain-Source On-State Resistance		R <sub>DS(ON)</sub>	$V_{GS}$ =10V, $I_D$ =20A		2.3	2.8	mΩ		
			V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A		4.2	5.4	mΩ		
DYNAMIC PARAMETERS									
Input Capacitance		$C_{ISS}$			4780	9500	pF		
Output Capacitance		Coss	$V_{GS}$ =0V, $V_{DS}$ =25V, f=1.0MHz		1365	2700	pF		
Reverse Transfer Capacitance		$C_{RSS}$			51	102	pF		
SWITCHING PARAMETERS									
Total Gate Charge (Note 1)		$Q_G$			59	120	nC		
Gate to Source Charge		$Q_{GS}$	V <sub>DS</sub> =48V, V <sub>GS</sub> =10V, I <sub>D</sub> =10A		10.4	20	nC		
Gate to Drain Charge		$Q_GD$			19.6	38	nC		
Turn-on Delay Time (Note 1)		$t_{D(ON)}$			22	44	ns		
Rise Time		$t_R$	$V_{DS}$ =30V, $V_{GS}$ =10V, $I_{D}$ =6.0A,		14	28	ns		
Turn-off Delay Time		t <sub>D(OFF)</sub>	$R_G=1.0\Omega$		40	80	ns		
Fall-Time		$t_{F}$			20	40	ns		
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS									
Maximum Body-Diode Continuous	Current	Is				100	Α		
Maximum Body-Diode Pulsed Curr	ent	I <sub>SM</sub>				200	Α		
Drain-Source Diode Forward Voltage	ge (Note 1)	$V_{SD}$	I <sub>S</sub> =1.0A, V <sub>GS</sub> =0V			1.0	V		

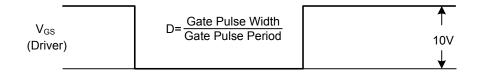
Notes: 1. Pulse Test: Pulse width ≤ 300µs, Duty cycle≤2%.

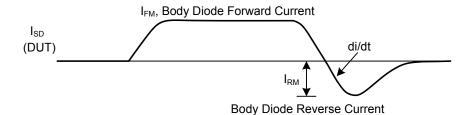
2. Essentially independent of operating temperature.

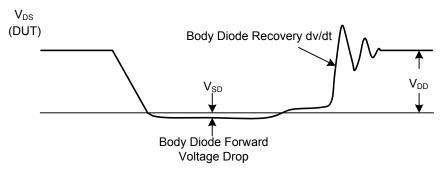
## ■ TEST CIRCUITS AND WAVEFORMS



#### Peak Diode Recovery dv/dt Test Circuit



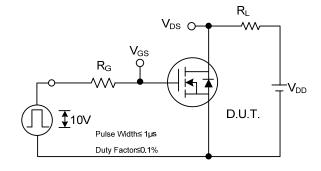


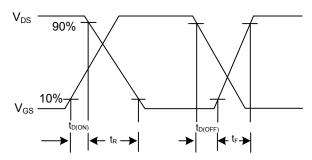


Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

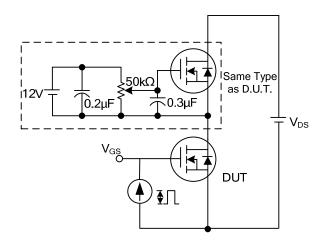
## **■ TEST CIRCUITS AND WAVEFORMS**

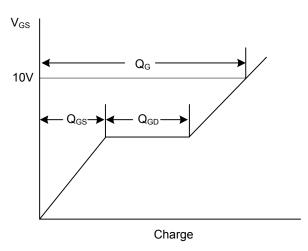




**Switching Test Circuit** 

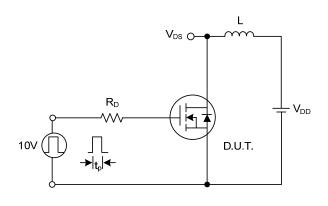
**Switching Waveforms** 

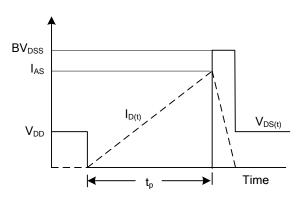




**Gate Charge Test Circuit** 

**Gate Charge Waveform** 

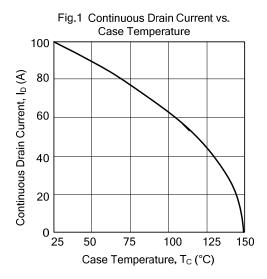


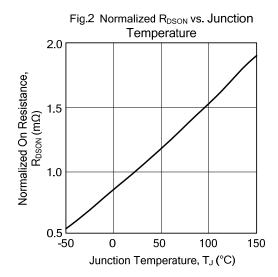


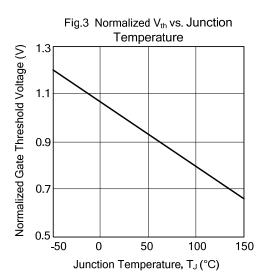
**Unclamped Inductive Switching Test Circuit** 

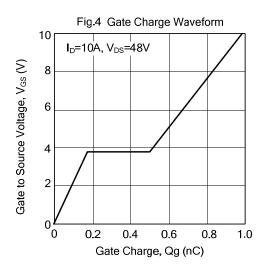
**Unclamped Inductive Switching Waveforms** 

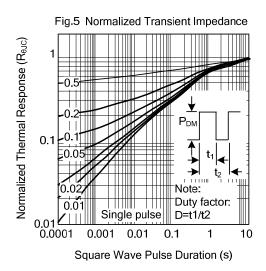
#### **■ TYPICAL CHARACTERISTICS**

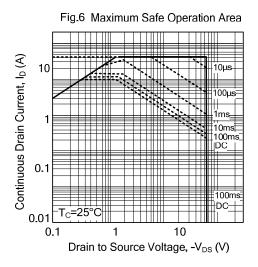












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