



**80N08-S**

*Power MOSFET*

**80A, 80V N-CHANNEL  
POWER MOSFET**

■ DESCRIPTION

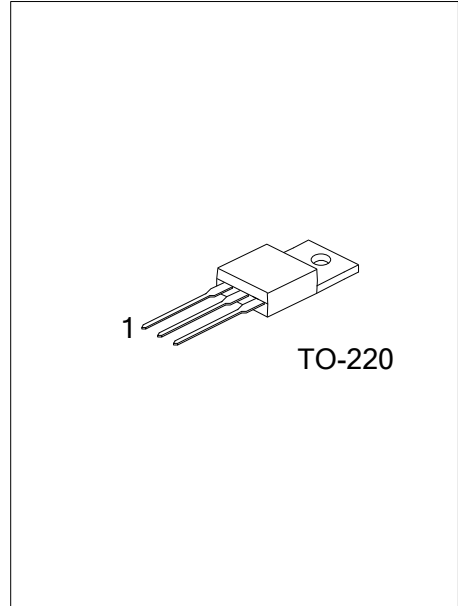
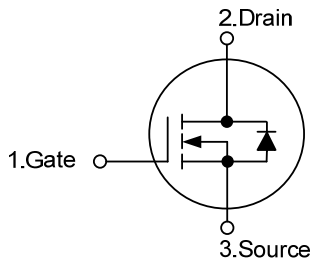
The UTC **80N08-S** is a N-channel MOSFET using UTC advanced technology.

The UTC **80N08-S** is suitable for power supply (secondary synchronous rectification), industrial and primary switch etc.

■ FEATURES

\*  $R_{DS(on)} < 18\text{ m}\Omega$  @  $V_{GS}=10V, I_D=40A$

■ SYMBOL



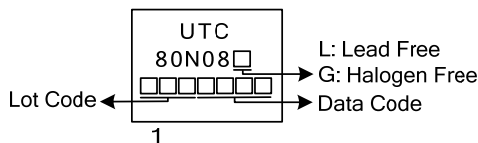
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
80N08L-TA3-T	80N08G-TA3-T	TO-220	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>80N08G-TA3-T</p> <p>(1)Packing Type (2)Package Type (3)Green Package</p>	<p>(1) T: Tube (2) TA3: TO-220 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ( $T_C=25^\circ\text{C}$ , unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{DSS}$	80	V
Gate-Source Voltage		$V_{GSS}$	$\pm 20$	V
Continuous Drain Current	Continuous	$I_D$	80	A
Pulsed Drain Current	Pulsed (Note 2)	$I_{DM}$	320	A
Avalanche Current (Note 3)		$I_{AR}$	91	A
Avalanche energy	Single Pulsed (Note 3)	$E_{AS}$	414	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	15	V/nS
Power Dissipation		$P_D$	200	W
Junction Temperature		$T_J$	+150	$^\circ\text{C}$
Storage Temperature Range		$T_{STG}$	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3.  $L=0.1\text{mH}$ ,  $I_{AS}=91\text{A}$ ,  $V_{DD}=50\text{V}$ ,  $R_G=25\Omega$ , Starting  $T_J = 25^\circ\text{C}$ .

4.  $I_{SD} \leq 30\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J = 25^\circ\text{C}$ .

■ THERMAL DATA

PARAMETER	SYMBOL	MAX	UNIT
Junction to Ambient	$\theta_{JA}$	62	$^\circ\text{C}/\text{W}$
Junction to Case	$\theta_{JC}$	0.75	$^\circ\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$I_D=1\text{mA}$ , $V_{GS}=0\text{V}$	80			V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=80\text{V}$ , $V_{GS}=0\text{V}$ , $T_J=25^\circ\text{C}$			1	$\mu\text{A}$
Gate-Source Leakage Current	$I_{GSS}$	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 20\text{V}$			$\pm 100$	nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	1.0		3.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$ , $I_D=40\text{A}$			18	m $\Omega$
<b>DYNAMIC PARAMETERS</b>						
Input Capacitance	$C_{ISS}$	$V_{GS}=0\text{V}$ , $V_{DS}=25\text{V}$ , $f=1.0\text{MHz}$		3550		pF
Output Capacitance	$C_{OSS}$			463		pF
Reverse Transfer Capacitance	$C_{RSS}$			36		pF
<b>SWITCHING PARAMETERS</b>						
Total Gate Charge (Note 1)	$Q_G$	$V_{DS}=50\text{V}$ , $I_D=1.3\text{A}$ , $V_{GS}=10\text{V}$ $I_G=100\mu\text{A}$ (Note 1, 2)		223		nC
Gate to Source Charge	$Q_{GS}$			15		nC
Gate to Drain Charge	$Q_{GD}$			19.2		nC
Turn-ON Delay Time (Note 1)	$t_{D(ON)}$	$V_{DD}=30\text{V}$ , $I_D=0.5\text{A}$ , $R_G=25\Omega$ , $V_{GS}=0\text{V}$ (Note 1, 2)		70		ns
Rise Time	$t_R$			73		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			1085		ns
Fall-Time	$t_F$			205		ns
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Maximum Body-Diode Continuous Current	$I_S$				80	A
Maximum Body-Diode Pulsed Current	$I_{SM}$				320	
Drain-Source Diode Forward Voltage (Note 1)	$V_{SD}$	$I_S=30\text{A}$ , $V_{GS}=0\text{V}$			1.3	V
Body Diode Reverse Recovery Time (Note 1)	$t_{rr}$	$I_S=30\text{A}$ , $V_{GS}=0\text{V}$		63.6		ns
Body Diode Reverse Recovery Charge	$Q_{rr}$	$di_F/dt=100\text{A}/\mu\text{s}$		164		nC

Note: 1. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

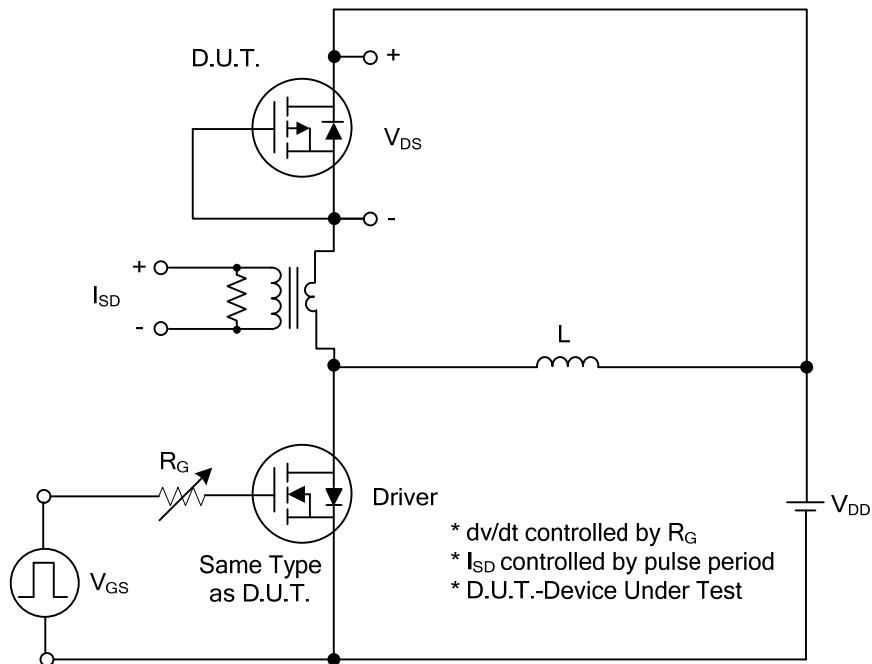


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

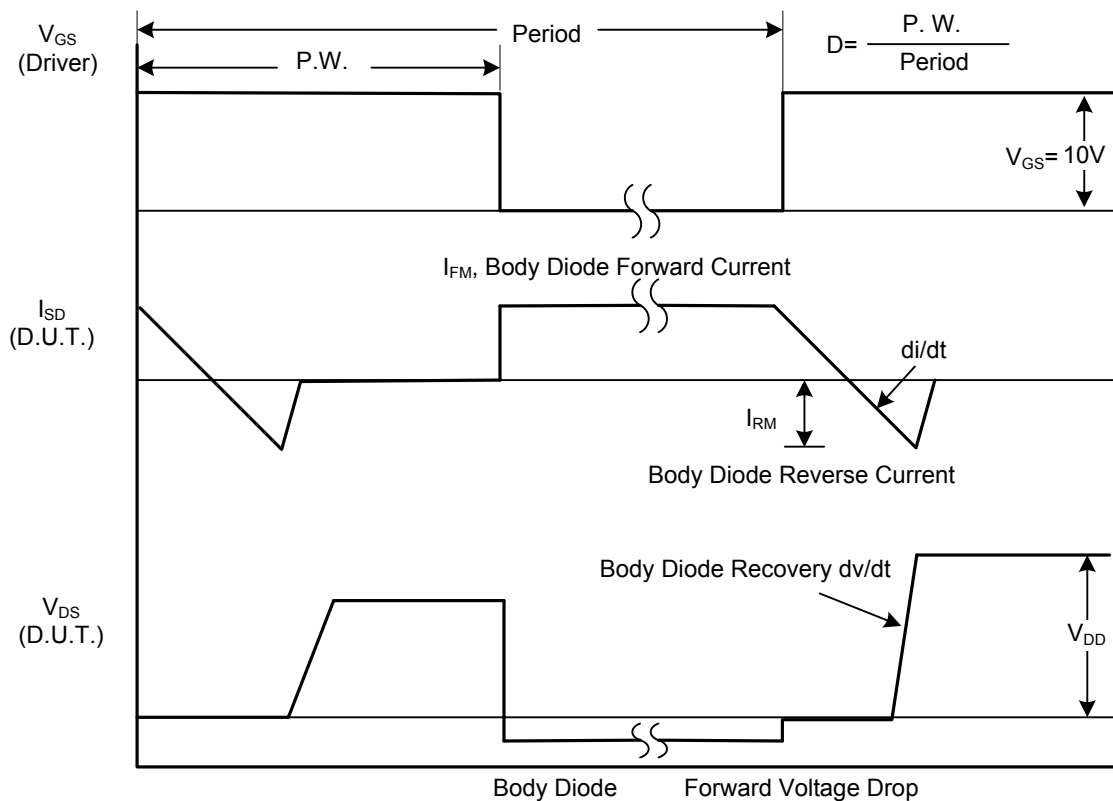
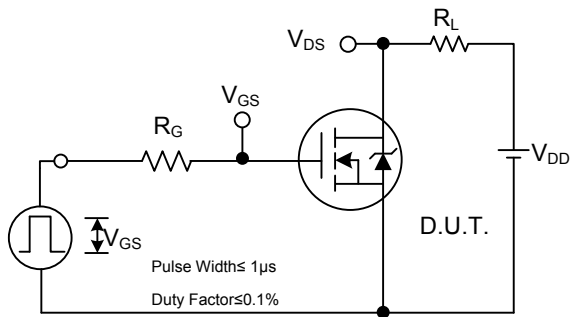
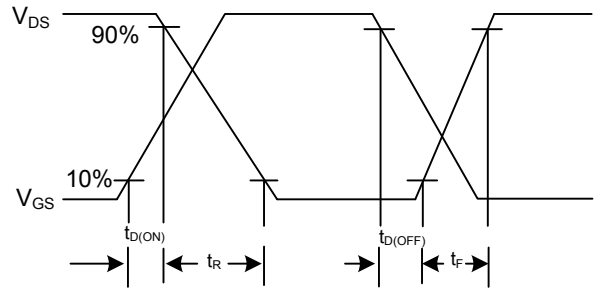


Fig. 1B Peak Diode Recovery dv/dt Waveforms

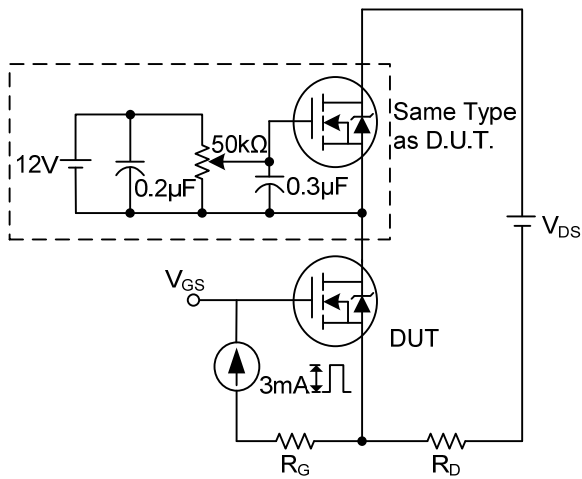
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



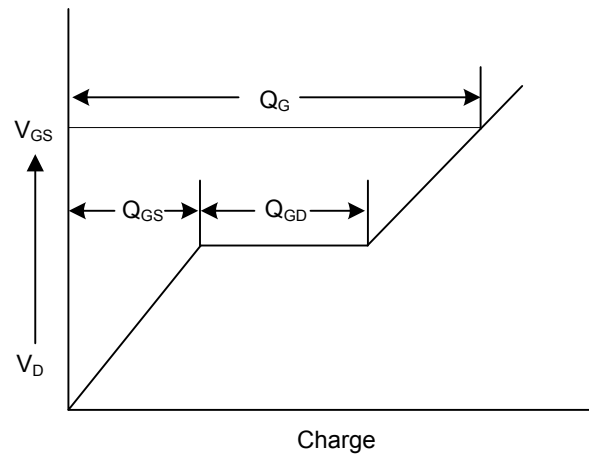
2A Switching Test Circuit



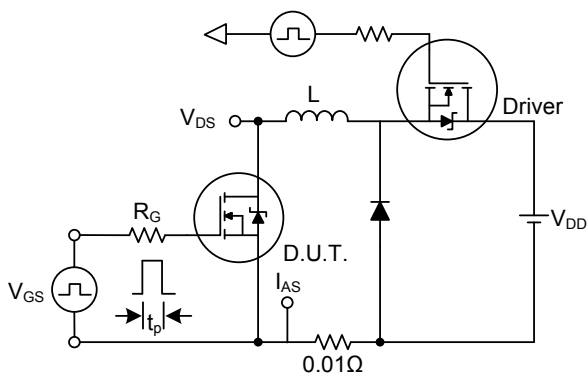
2B Switching Waveforms



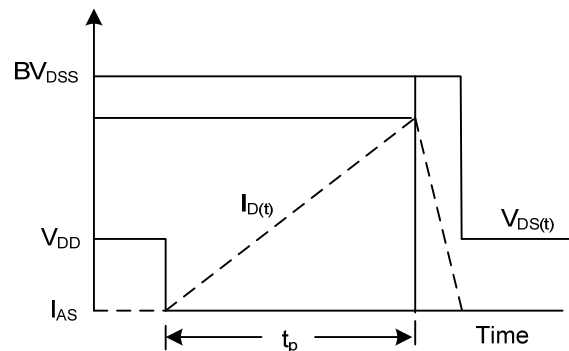
3A Gate Charge Test Circuit



3B Gate Charge Waveform



4A Unclamped Inductive Switching Test Circuit



4B Unclamped Inductive Switching Waveforms

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