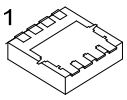
UND02R100L

Preliminary ***POWER MOSFET***

25A, 20V N-CHANNEL ENHANCEMENT MODE TRENCH POWER MOSFET



PDFN3×3

■ DESCRIPTION

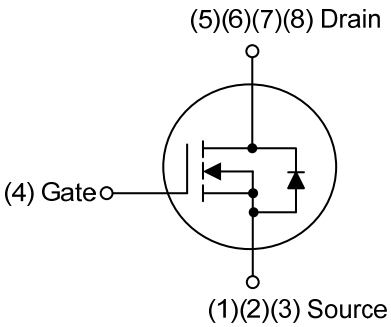
The UTC **UND02R100L** is an N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with low Rdson characteristic by high cell density trench technology.

The UTC **UND02R100L** is suitable for high efficiency synchronous rectification in SMPS, UPS, hard switched and high frequency circuits.

■ FEATURES

* $R_{DS(ON)}$ ≤ 8.2 mΩ @ V_{GS}=4.5V, I_D=8.0A
  $R_{DS(ON)}$ ≤ 9.5 mΩ @ V_{GS}=2.5V, I_D=7.0A
  $R_{DS(ON)}$ ≤ 12 mΩ @ V_{GS}=1.8V, I_D=4.0A
* High Cell Density Trench Technology
* High Power and Current Handling Capability

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UND02R100LK-P3030-R	UND02R100LG-P3030-R	PDFN3×3	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UND02R100LG-P3030-R

(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) P3030: PDFN3×3
(3) G: Halogen Free and Lead Free, K: Lead Free

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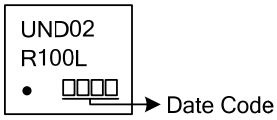
■ MARKING



■ ABSOLUTE MAXIMUM RATING (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	20	V
Gate-Source Voltage		V_{GSS}	±8	V
Drain Current	Continuous	I_D	25	A
	Pulsed (Note 2)	I_{DM}	60	A
Power Dissipation		P_D	31	W
Junction Temperature		T_J	+150	°C
Storage Temperature Range		T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature.

■ THERMAL RESISTANCES CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	40	°C/W
Junction to Case	θ_{JC}	4	°C/W

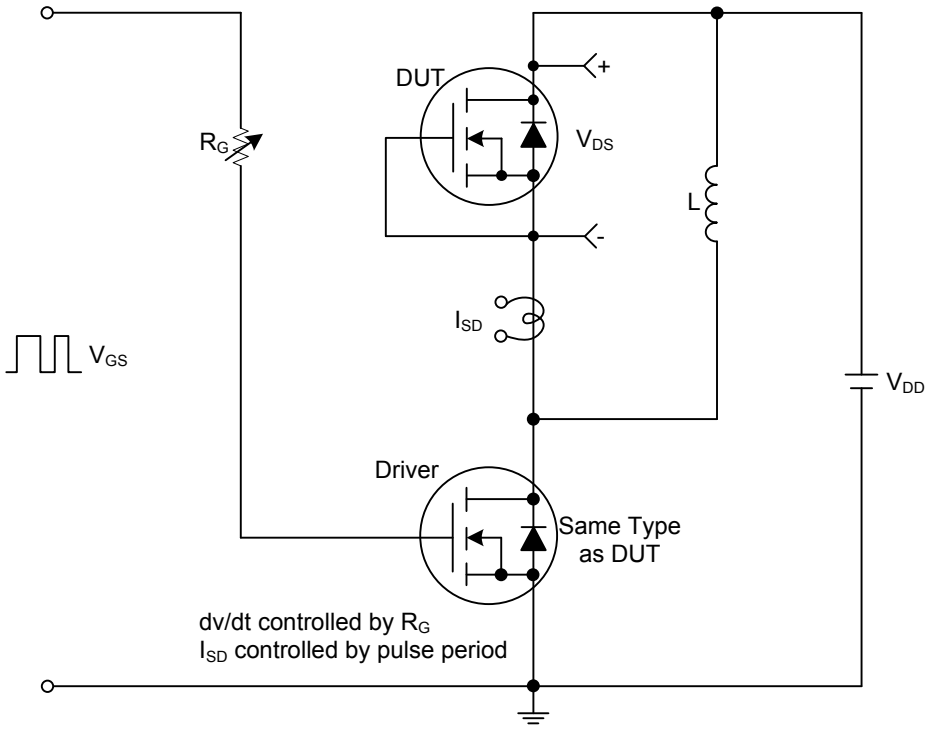
Note: Surface mounted on 1×1 FR4 board.

■ ELECTRICAL CHARACTERISTICS (T_J =25°C, unless otherwise specified)

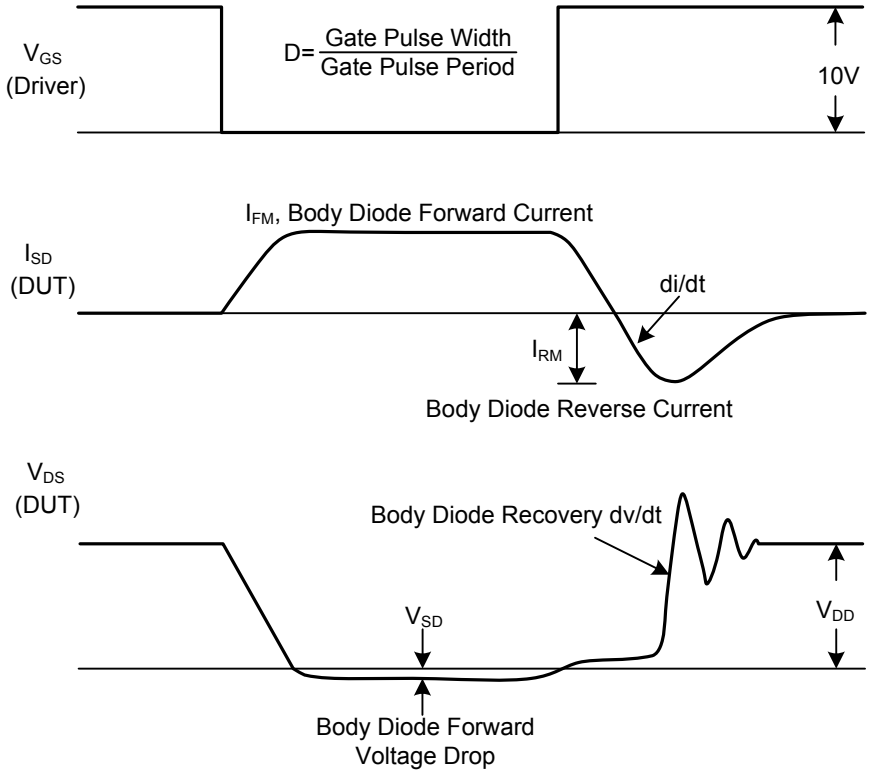
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	I_D=250μA, V_{GS}=0V	20			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=20V, V_{GS}=0V			1	μA
Gate-Source Leakage Current	Forward	I_{GSS}	V_{GS}=+8V, V_{DS}=0V			+100	nA
	Reverse		V_{GS}=-8V, V_{DS}=0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	0.4		0.9	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=4.5V, I_D=8.0A		6.6	8.2	mΩ
			V_{GS}=2.5V, I_D=7.0A		7.7	9.5	mΩ
			V_{GS}=1.8V, I_D=4.0A		9.6	12	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	V_{GS}=0V, V_{DS}=10V, f=1.0MHz		2705		pF
Output Capacitance		C_{OSS}			241		pF
Reverse Transfer Capacitance		C_{RSS}			205		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q_G	V_{DS}=10V, V_{GS}=4.5V, I_D=10A, I_G=100μA (Note 1, 2)		66.8		nC
Gate to Source Charge		Q_{GS}			3.2		nC
Gate to Drain Charge		Q_{GD}			4.8		nC
Turn-on Delay Time (Note 1)		$t_{D(ON)}$	V_{DD}=10V, V_{GS}=4.5V, I_D=10A, R_G =1Ω (Note 1, 2)		58		ns
Rise Time		t_R			61		ns
Turn-off Delay Time		$t_{D(OFF)}$			450		ns
Fall-Time		t_F			330		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				25	A
Maximum Body-Diode Pulsed Current		I_{SM}				60	A
Drain-Source Diode Forward Voltage (Note 1)		V_{SD}	I_S=10A, V_{GS}=0V		0.8	1.2	V
Reverse Recovery Time (Note 1)		t_{rr}	I_S=10A, V_{GS}=0V, dI_F/dt =100A/μs		2.08		μS
Reverse Recovery Charge		Q_{rr}			18.3		μC

Notes: 1. Pulse Test : Pulse width ≤ 200μs, Duty cycle ≤ 2%.
2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS



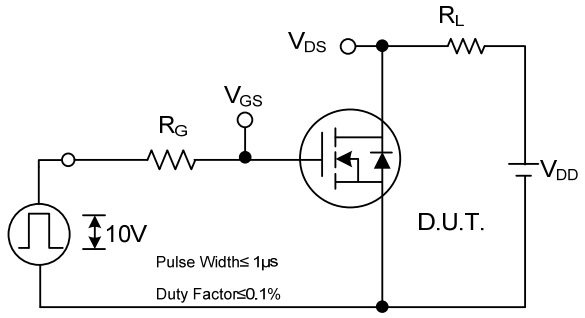
Peak Diode Recovery dv/dt Test Circuit



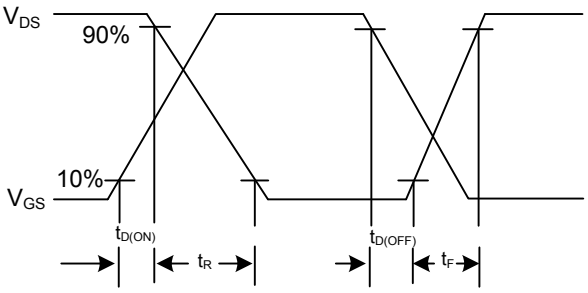
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

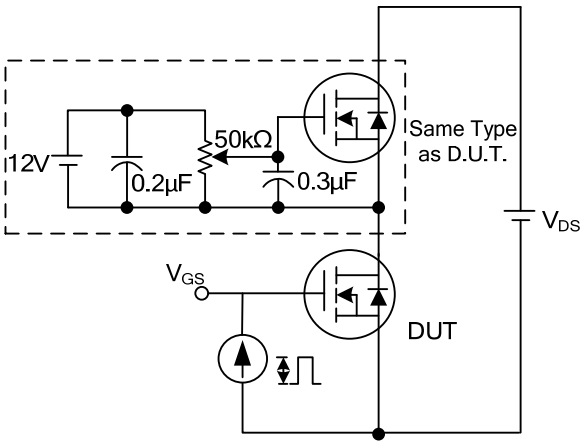
■ TEST CIRCUITS AND WAVEFORMS



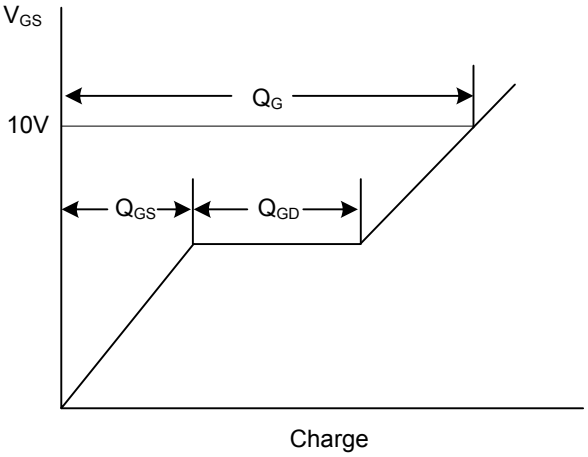
Switching Test Circuit



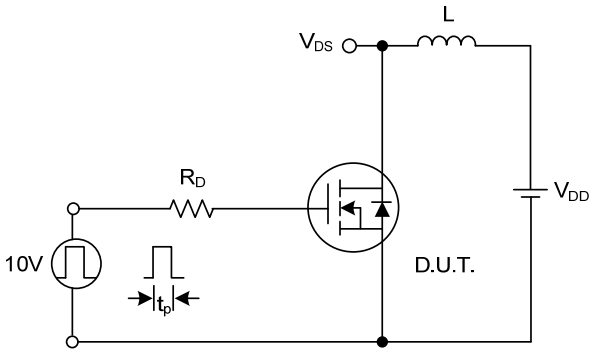
Switching Waveforms



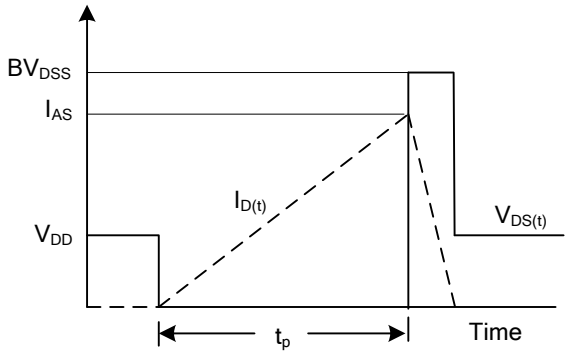
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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