



## UF3205-S

Power MOSFET

### 110A, 55V N-CHANNEL POWER MOSFET

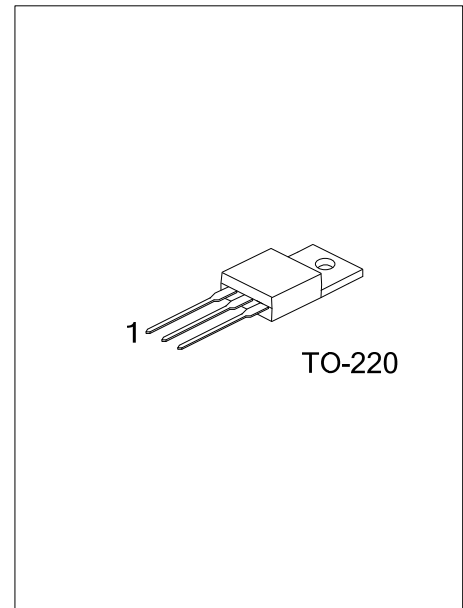
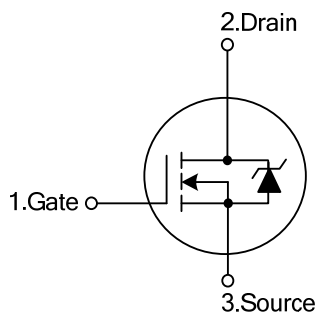
#### DESCRIPTION

The UTC **UF3205-S** uses advanced technology to provide excellent  $R_{DS(ON)}$ , fast switching, low gate charge, and extremely efficient. This device is suitable for all commercial-industrial applications at power dissipation levels to approximately 50 watts.

#### FEATURES

- \*  $R_{DS(ON)} < 9.0\ m\Omega$  @  $V_{GS}=10V, I_D=62A$
- \* Fast Switching Capability
- \* Avalanche Energy Specified
- \* Improved  $dv/dt$  Capability, High Ruggedness

#### SYMBOL



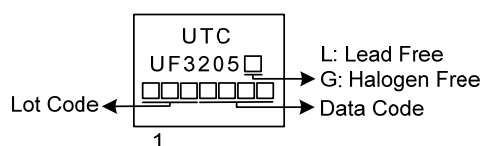
#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UF3205L-TA3-T	UF3205G-TA3-T	TO-220	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UF3205G-TA3-T</p> <p>(1)Packing Type (2)Package Type (3)Green Package</p>	<p>(1) T: Tube (2) TA3: TO-220 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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#### MARKING



■ ABSOLUTE MAXIMUM RATINGS ( $T_C=25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Drain-Source Voltage		$V_{DS}$	55	V
Drain Current	Continuous ( $V_{GS}=10\text{V}$ )	$I_D$	110	A
	Pulsed (Note 2)	$I_{DM}$	440	
Avalanche Energy	Single Pulsed (Note 3)	$E_{AS}$	335	mJ
Peak Diode Recovery $dv/dt$ (Note 4)		$dv/dt$	9	V/ns
Power Dissipation		$P_D$	200	W
Junction Temperature		$T_J$	+150	$^{\circ}\text{C}$
Storage Temperature		$T_{STG}$	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3.  $L=0.13\text{mH}$ ,  $I_{AS}=62\text{A}$ ,  $V_{DD}=-50\text{V}$ ,  $R_G=25\Omega$ , Starting  $T_J=25^{\circ}\text{C}$

4.  $I_{SD}\leq 62\text{A}$ ,  $di/dt \leq 200\mu\text{A/s}$ ,  $V_{DD}\leq BV_{DSS}$ , Starting  $T_J=25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	MAX	UNIT
Junction to Ambient	$\theta_{JA}$	62.5	$^{\circ}\text{C/W}$
Junction to Case	$\theta_{JC}$	0.75	$^{\circ}\text{C/W}$

■ ELECTRICAL CHARACTERISTICS ( $T_J = 25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0\text{V}$ , $I_D=250\mu\text{A}$	55			V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=55\text{V}$ , $V_{GS}=0\text{V}$			1	$\mu\text{A}$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20\text{V}$ , $V_{DS}=0\text{V}$			$\pm 100$	nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	1.0		3.0	V
Static Drain-Source On-Resistance (Note)	$R_{DS(ON)}$	$V_{GS}=10\text{V}$ , $I_D=62\text{A}$			9.0	m $\Omega$
<b>DYNAMIC PARAMETERS</b>						
Input Capacitance	$C_{ISS}$	$V_{DS}=25\text{V}$ , $V_{GS}=0\text{V}$ , $f=1\text{MHz}$		3280		pF
Output Capacitance	$C_{OSS}$			685		pF
Reverse Transfer Capacitance	$C_{RSS}$			95		pF
<b>SWITCHING PARAMETERS</b>						
Total Gate Charge	$Q_G$	$V_{DS}=50\text{V}$ , $I_D=1.3\text{A}$ , $V_{GS}=10\text{V}$		287		nC
Gate Source Charge	$Q_{GS}$			12		nC
Gate Drain Charge	$Q_{GD}$			27		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=30\text{V}$ , $I_D=0.5\text{A}$ , $R_G=25\Omega$ , $V_{GS}=10\text{V}$ (Note)		70		ns
Turn-ON Rise Time	$t_R$			126		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			1100		ns
Turn-OFF Fall-Time	$t_F$			368		ns
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Maximum Continuous Drain-Source Diode Forward Current	$I_S$				110	A
Maximum Pulsed Drain-Source Diode Forward Current	$I_{SM}$				440	A
Diode Forward Voltage	$V_{SD}$	$I_S=62\text{A}$ , $V_{GS}=0\text{V}$			1.3	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F=30\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$ (Note)		68		ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			0.14		$\mu\text{C}$

Notes: 1. Pulse Test : Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$ .

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

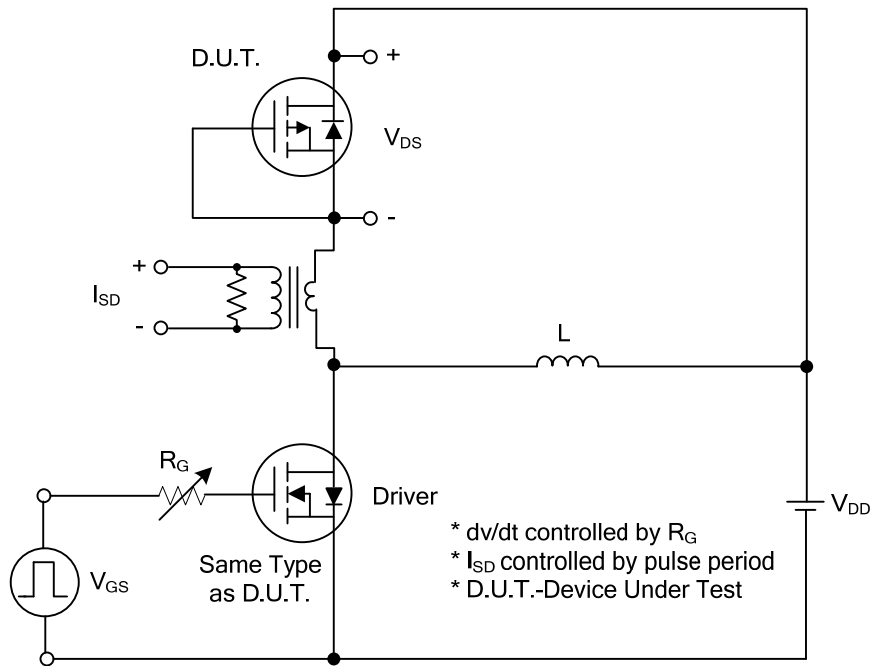


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

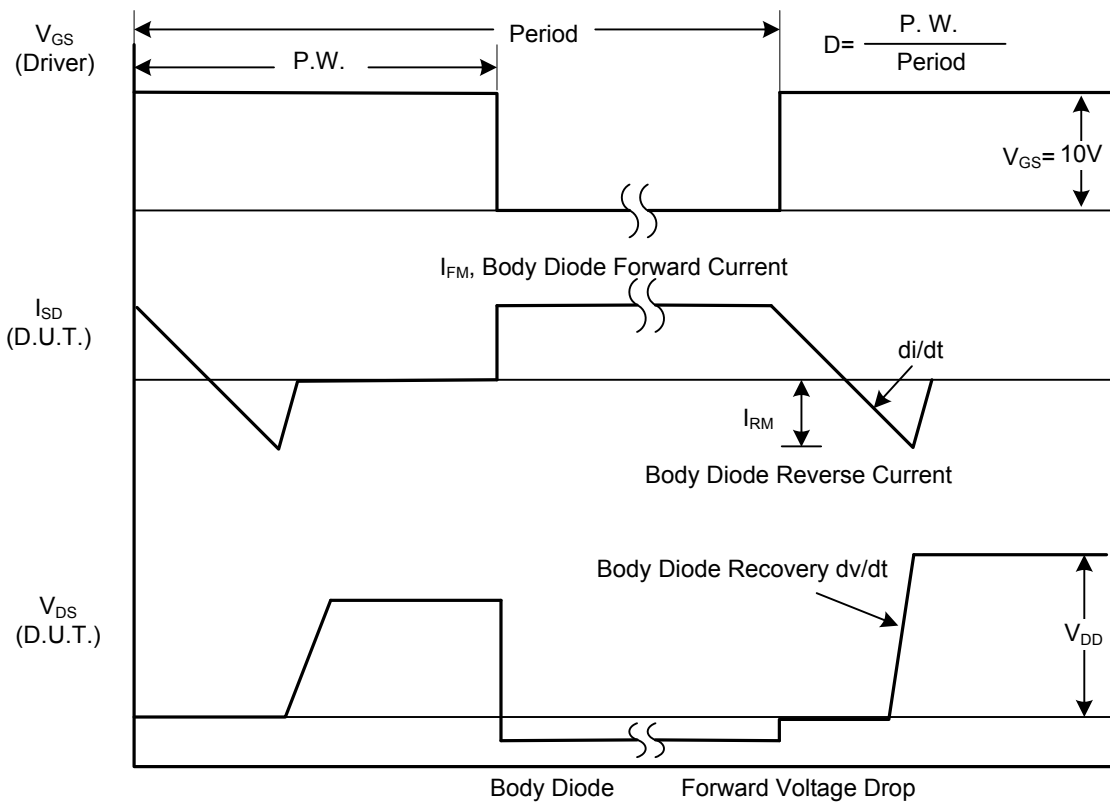
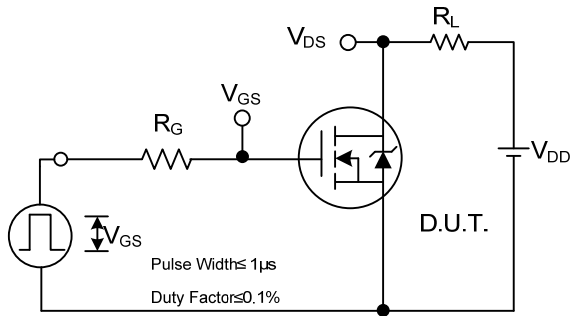
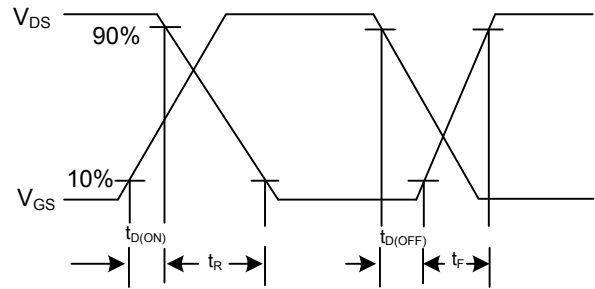


Fig. 1B Peak Diode Recovery dv/dt Waveforms

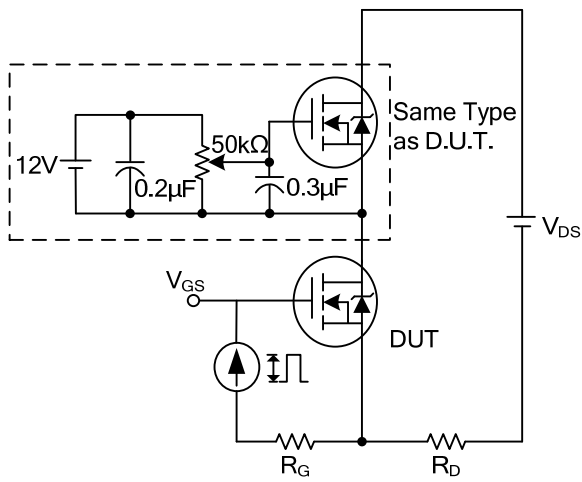
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



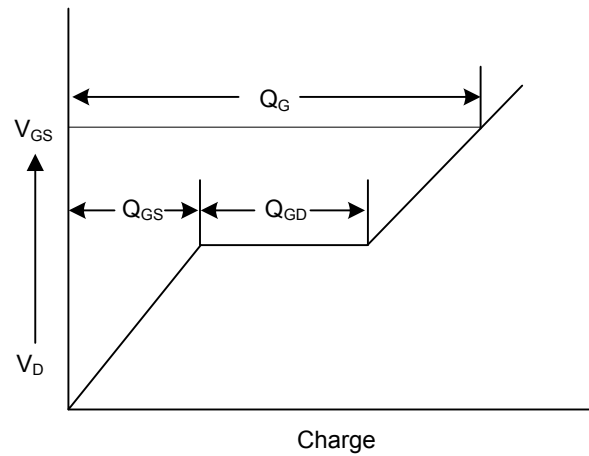
2A Switching Test Circuit



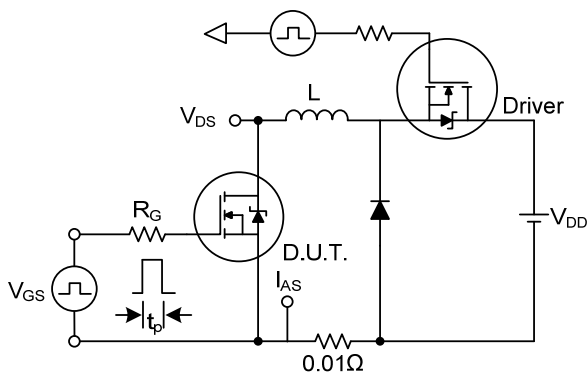
2B Switching Waveforms



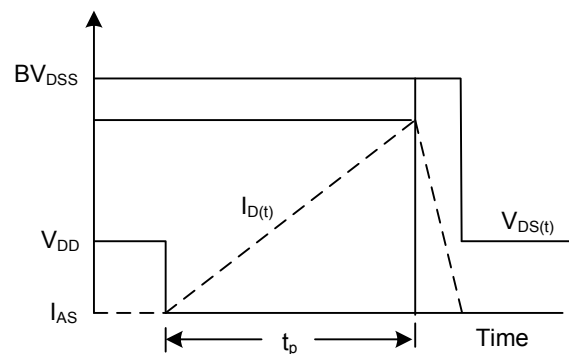
3A Gate Charge Test Circuit



3B Gate Charge Waveform

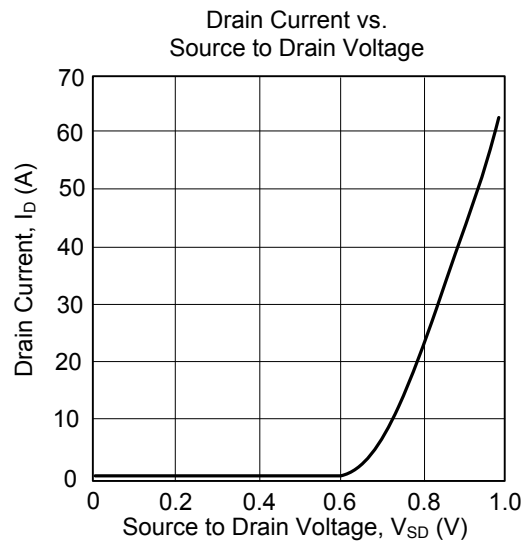
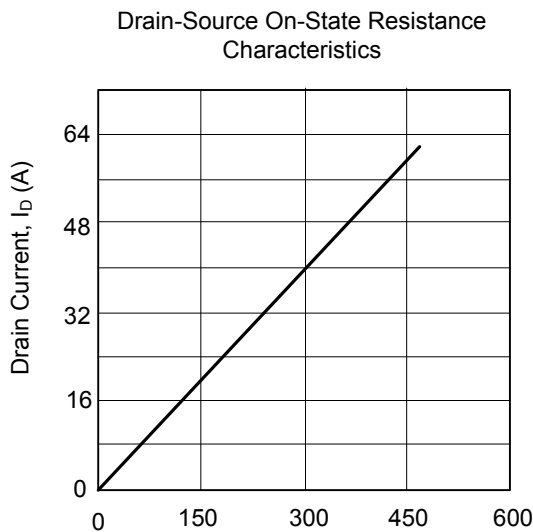
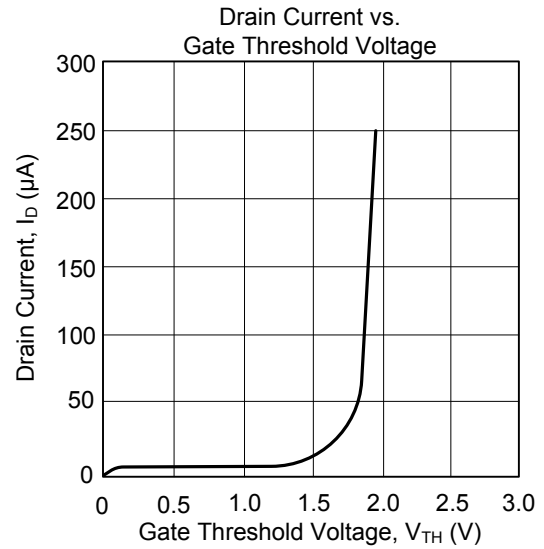
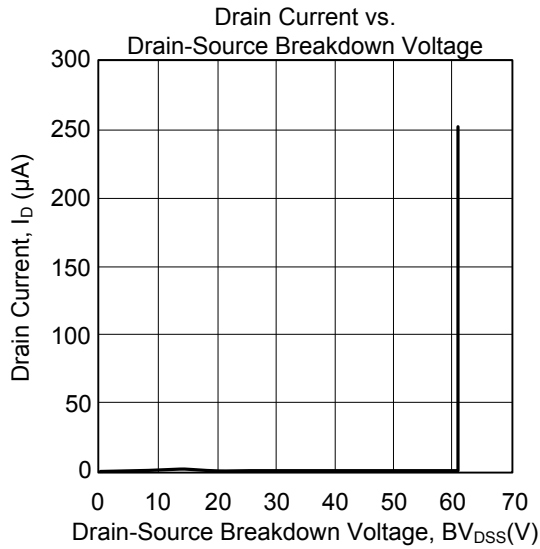


4A Unclamped Inductive Switching Test Circuit



4B Unclamped Inductive Switching Waveforms

### ■ TYPICAL CHARACTERISTICS



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