



## 7A, 800V N-CHANNEL POWER MOSFET

### DESCRIPTION

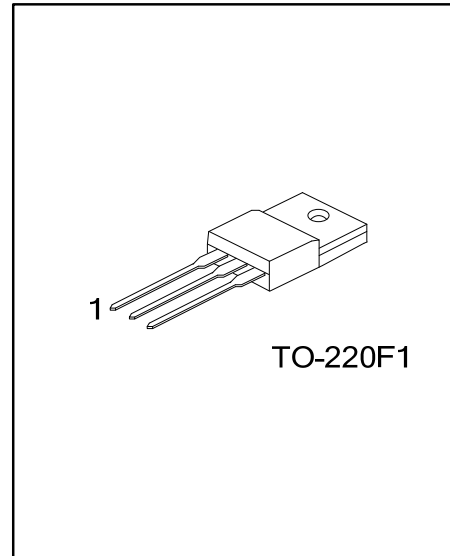
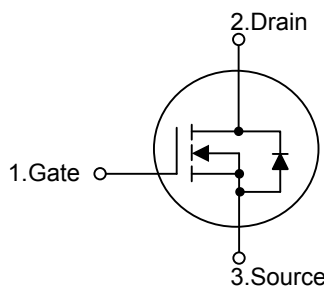
The UTC **7N80-CS** is a N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology specialized in allowing a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **7N80-CS** is universally applied in high efficiency switch mode power supply.

### FEATURES

- \*  $R_{DS(on)} < 2.0\Omega @ V_{GS}=10V, I_D=3.5A$
- \* Improved dv/dt capability
- \* Fast switching
- \* 100% avalanche tested

### SYMBOL



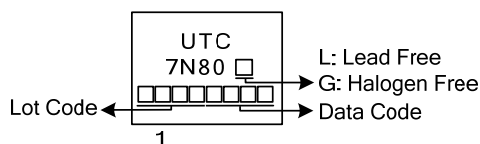
### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
7N80L-TF1-T	7N80G-TF1-T	TO-220F1	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>7N80G-TF1-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) T: Tube</p> <p>(2) TF1: TO-220F1</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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### MARKING



■ ABSOLUTE MAXIMUM RATINGS ( $T_C=25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	$V_{DSS}$	800	V
Gate-Source Voltage	$V_{GSS}$	$\pm 30$	V
Drain Current (Note 2)	Continuous	$I_D$	7
	Pulsed	$I_{DM}$	28
Avalanche Energy	Single Pulsed (Note 3)	$E_{AS}$	265
Peak Diode Recovery dv/dt (Note 4)	dv/dt	1.08	V/ns
Power Dissipation	$P_D$	51	W
Junction Temperature	$T_J$	+150	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-55~+150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3.  $L = 24\text{mH}$ ,  $I_{AS} = 4.7\text{A}$ ,  $V_{DD} = 50\text{V}$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$

4.  $I_{SD} \leq 7\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	$\theta_{JA}$	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	$\theta_{JC}$	2.45	$^\circ\text{C}/\text{W}$

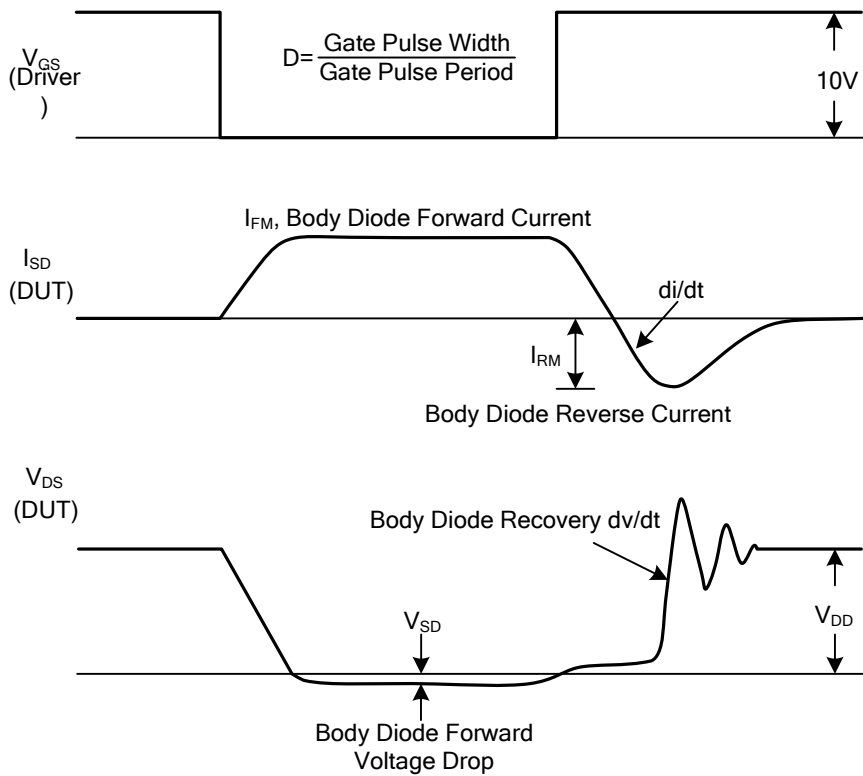
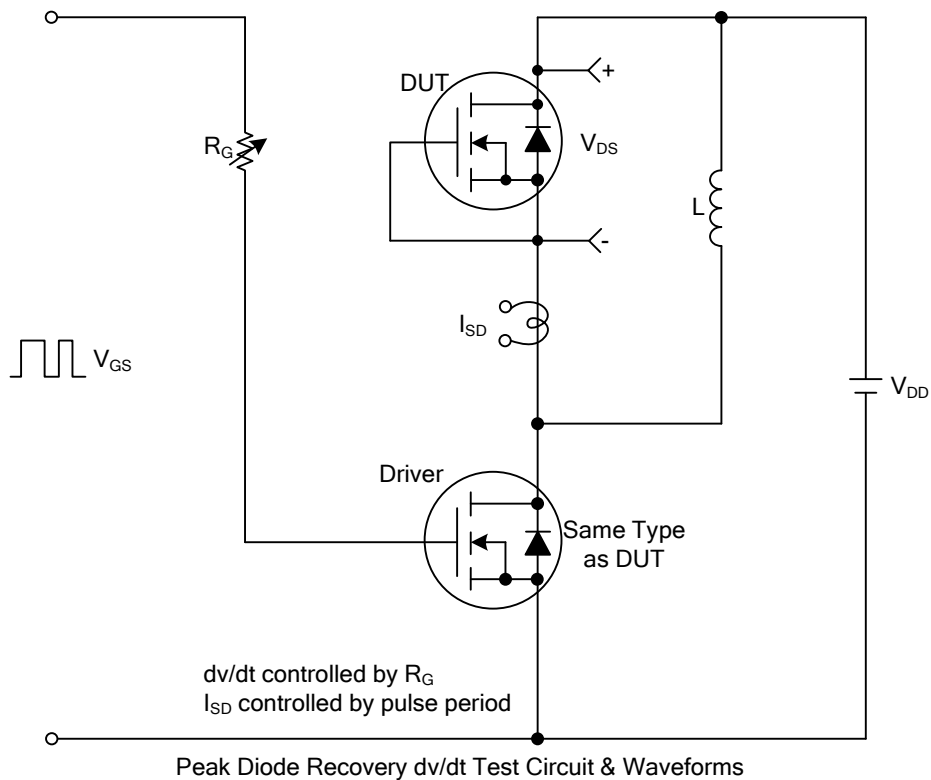
■ ELECTRICAL CHARACTERISTICS ( $T_J=25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>OFF CHARACTERISTICS</b>							
Drain-Source Breakdown Voltage	$BV_{DSS}$	$I_D=250\mu\text{A}$ , $V_{GS}=0\text{V}$	800			V	
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=800\text{V}$ , $V_{GS}=0\text{V}$			10	$\mu\text{A}$	
		$V_{DS}=640\text{V}$ , $T_C=125^\circ\text{C}$			100		
Gate- Source Leakage Current	Forward	$I_{GSS}$			100	nA	
	Reverse						$V_{GS}=-30\text{V}$ , $V_{DS}=0\text{V}$
<b>ON CHARACTERISTICS</b>							
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	3.0		5.0	V	
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$ , $I_D=3.5\text{A}$			2.0	$\Omega$	
<b>DYNAMIC PARAMETERS</b>							
Input Capacitance	$C_{ISS}$	$V_{GS}=0\text{V}$ , $V_{DS}=25\text{V}$ , $f=1.0\text{MHz}$		700		pF	
Output Capacitance	$C_{OSS}$				110		pF
Reverse Transfer Capacitance	$C_{RSS}$				15		pF
<b>SWITCHING PARAMETERS</b>							
Total Gate Charge	$Q_G$	$V_{DS}=50\text{V}$ , $I_D=1.3\text{A}$ $I_g=100\mu\text{A}$ (Note 1, 2)		74		nC	
Gate to Source Charge	$Q_{GS}$			9		nC	
Gate to Drain Charge	$Q_{GD}$			12		nC	
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=400\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=0.5\text{A}$ , $R_G=25\Omega$ (Note 1, 2)		66		ns	
Rise Time	$t_R$			82		ns	
Turn-OFF Delay Time	$t_{D(OFF)}$			218		ns	
Fall-Time	$t_F$			46		ns	
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>							
Maximum Body-Diode Continuous Current	$I_S$				7	A	
Maximum Body-Diode Pulsed Current	$I_{SM}$				28	A	
Drain-Source Diode Forward Voltage	$V_{SD}$	$I_S=7\text{A}$ , $V_{GS}=0\text{V}$			1.4	V	
Reverse Recovery Time	$t_{rr}$	$I_S=7\text{A}$ , $V_{GS}=0\text{V}$ , $dI_F/dt=100\text{A}/\mu\text{s}$ (Note 1)		740		ns	
Reverse Recovery Charge	$Q_{rr}$			4.4		$\mu\text{C}$	

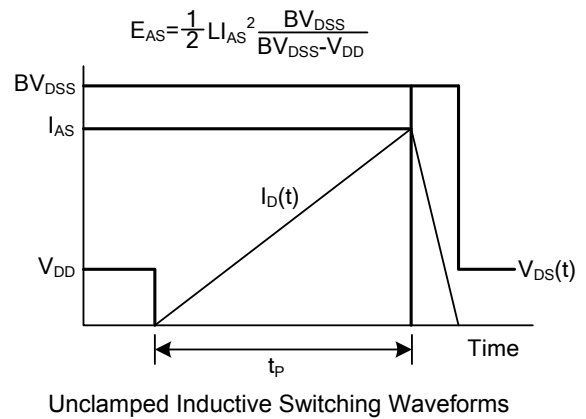
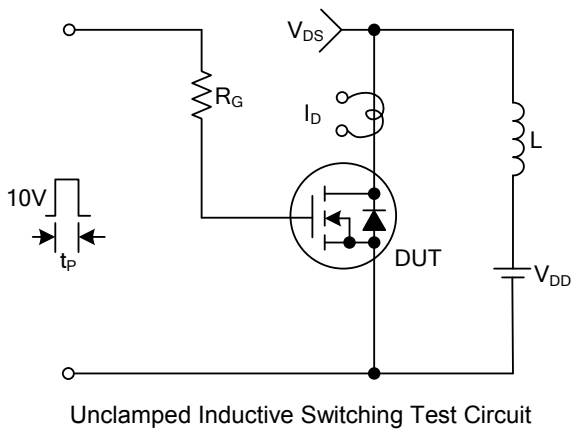
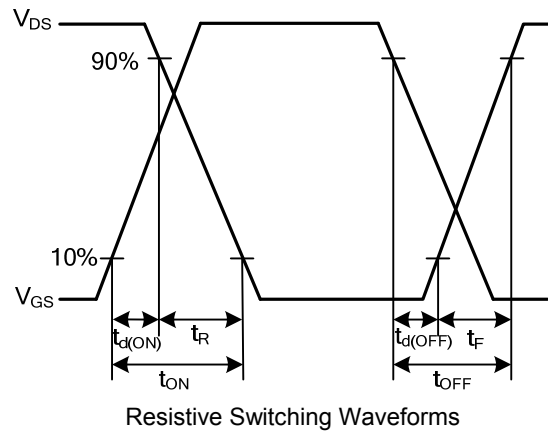
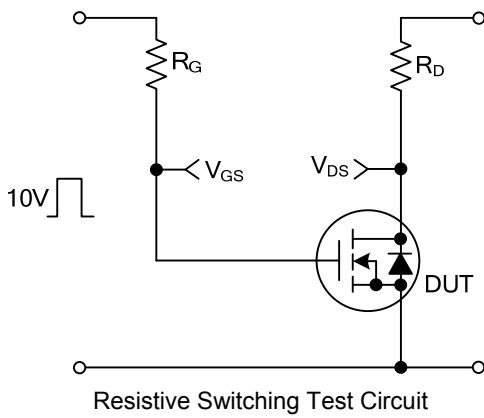
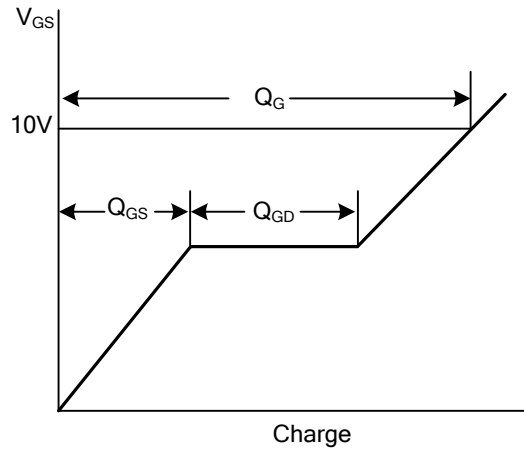
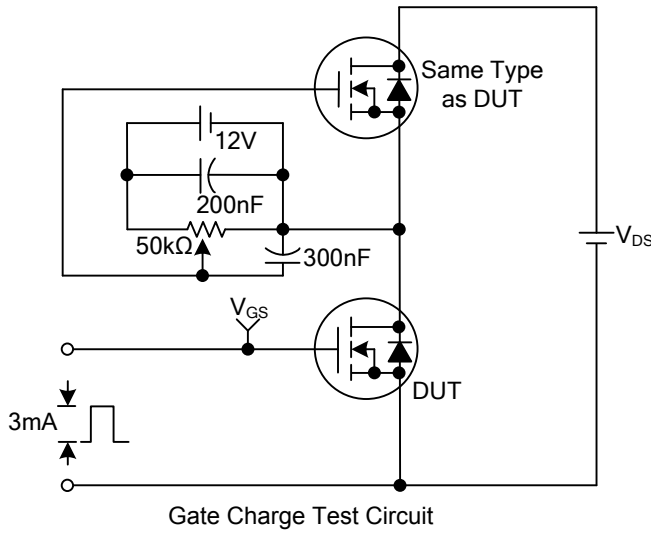
Notes: 1. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$ .

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



■ TEST CIRCUITS AND WAVEFORMS (Cont.)



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