



UT2309-H

Preliminary

Power MOSFET

**-3.7A, -30V P-CHANNEL
ENHANCEMENT MODE
POWER MOSFET**

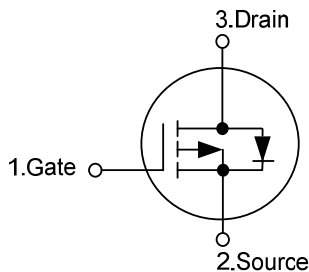
■ DESCRIPTION

The UTC **UT2309-H** is P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

■ FEATURES

- * $R_{DS(ON)} < 75\text{ m}\Omega$ @ $V_{GS} = -10V, I_D = -3.0A$
- $R_{DS(ON)} < 120\text{ m}\Omega$ @ $V_{GS} = -4.5V, I_D = -2.0A$
- * Extremely low on-resistance due to high density cell
- * Perfect thermal performance and electrical capability with advanced technology of trench process

■ SYMBOL

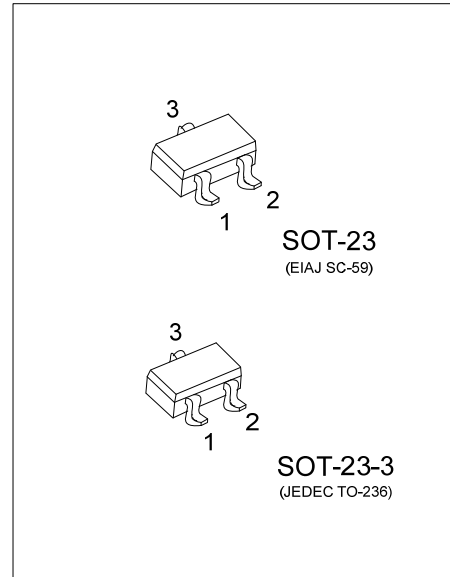


■ ORDERING INFORMATION

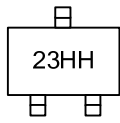
Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT2309L-AE2-R	UT2309G-AE2-R	SOT-23-3	G	S	D	Tape Reel
UT2309L-AE3-R	UT2309G-AE3-R	SOT-23	G	S	D	Tape Reel

Note: Pin Assignment: G: Gate S: Source D: Drain

<p>UT2309G-AE2-R</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) R: Tape Reel (2) AE2: SOT-23-3, AE3: SOT-23 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
---	--



■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	-30	V
Gate-Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current	I_D	-3.7	A
Pulsed Drain Current	I_{DM}	-14.8	A
Power Dissipation	P_D	1.38	W
Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient (PCB mounted)	θ_{JA}	90	$^\circ\text{C}/\text{W}$

Note: The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

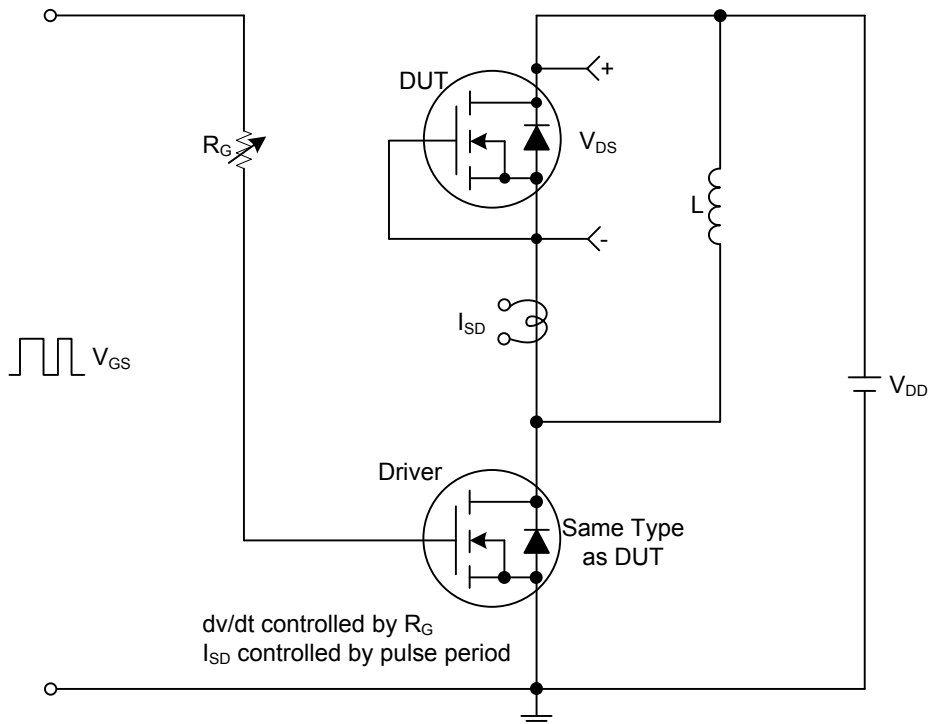
■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0\text{V}, I_D=-250\mu\text{A}$	-30			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=-30\text{V}, V_{GS}=0\text{V}, T_J=25^\circ\text{C}$			-1	μA
		$V_{DS}=-24\text{V}, V_{GS}=0\text{V}, T_J=125^\circ\text{C}$			-10	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$			± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	-1.2		-2.5	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10\text{V}, I_D=-3.0\text{A}$			75	m Ω
		$V_{GS}=-4.5\text{V}, I_D=-2.0\text{A}$			120	m Ω
DYNAMIC PARAMETERS^b						
Input Capacitance	C_{ISS}	$V_{DS}=-25\text{V}, V_{GS}=0\text{V}, f=1.0\text{MHz}$		425		pF
Output Capacitance	C_{OSS}			53		pF
Reverse Transfer Capacitance	C_{RSS}			45		pF
SWITCHING PARAMETERS^b						
Total Gate Charge (Note 1)	Q_G	$V_{DS}=-10\text{V}, V_{GS}=-4.5\text{V}, I_D=-3.0\text{A}$		24		nC
Gate Source Charge	Q_{GS}			4		nC
Gate Drain Charge	Q_{GD}			5		nC
Turn-ON Delay Time (Note 1)	$t_{D(ON)}$	$V_{DS}=-10\text{V}, V_{GS}=-4.5\text{V}, I_D=-1.0\text{A}$ $R_G=10\Omega$		30		ns
Turn-ON Rise Time	t_R			68		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			106		ns
Turn-OFF Fall-Time	t_F			186		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S	$V_G=V_D=0\text{V}$, Force Current			-3.7	A
Maximum Body-Diode Pulsed Current	I_{SM}				-14.8	A
Drain-Source Diode Forward Voltage	V_{SD}	$I_S=-3.7\text{A}, V_{GS}=0\text{V}, T_J=25^\circ\text{C}$			1.4	V

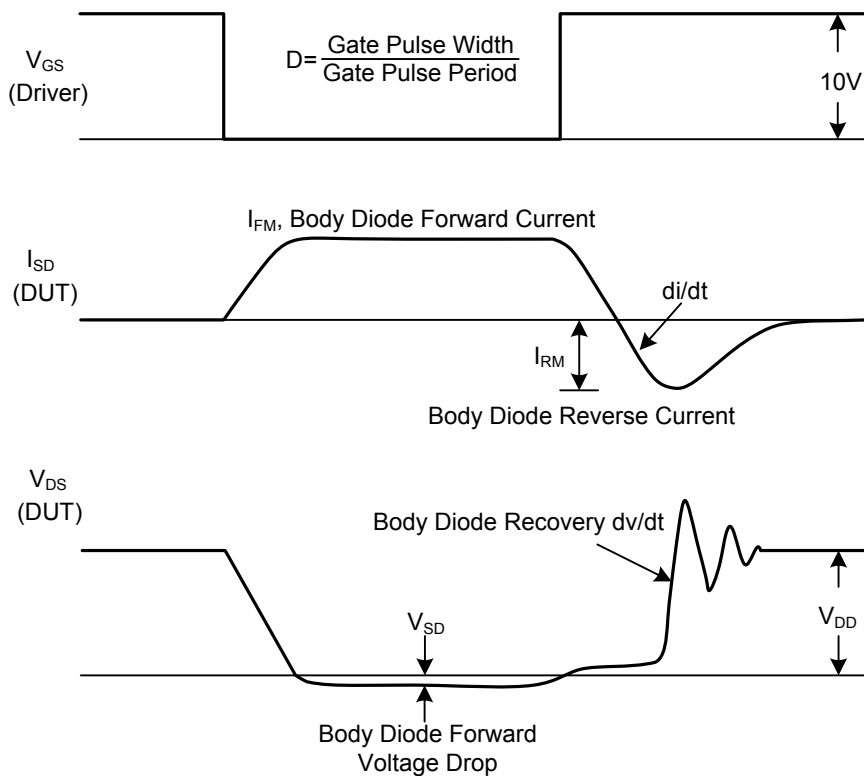
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



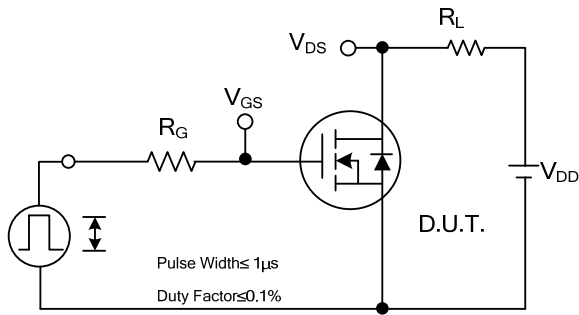
Peak Diode Recovery dv/dt Test Circuit



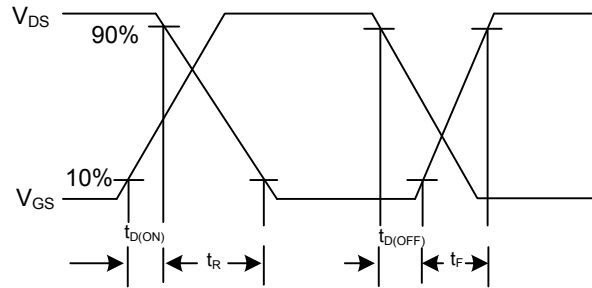
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

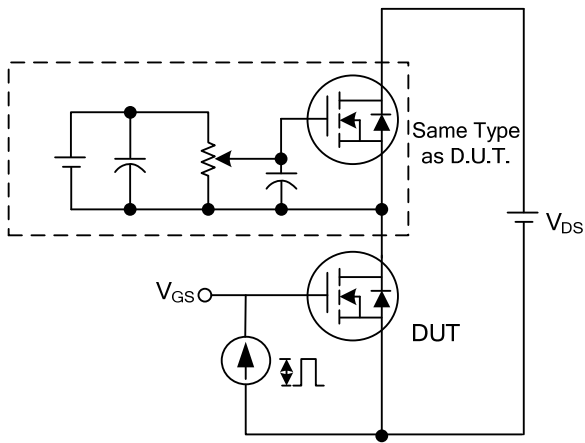
■ TEST CIRCUITS AND WAVEFORMS



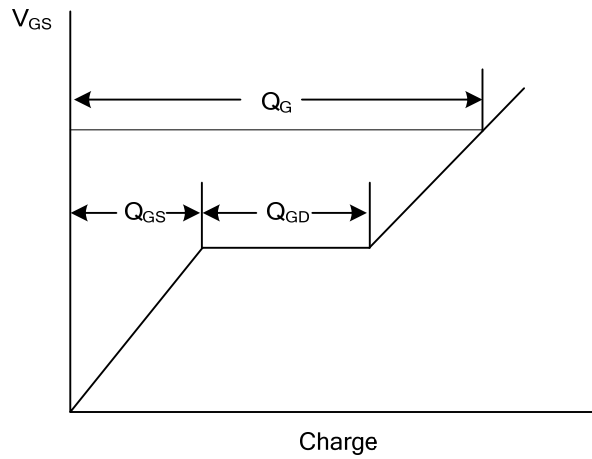
Switching Test Circuit



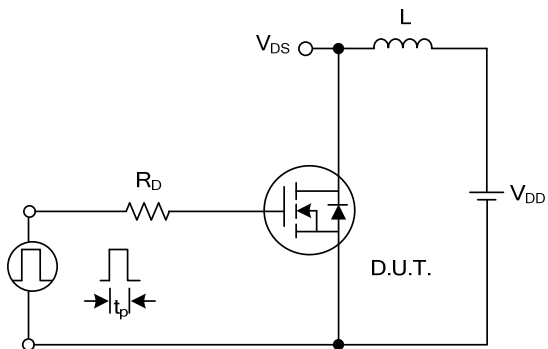
Switching Waveforms



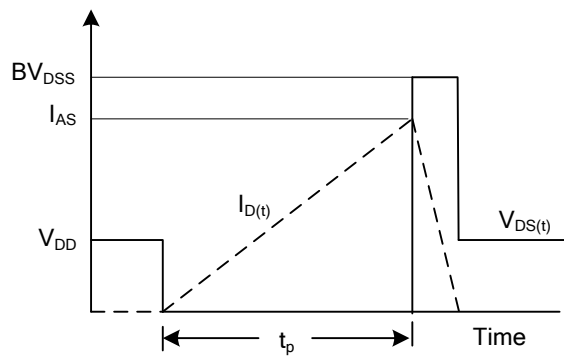
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. UTC reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.