



UF7464

Power MOSFET

3A, 200V N-CHANNEL ENHANCEMENT MODE TRENCH POWER MOSFET

DESCRIPTION

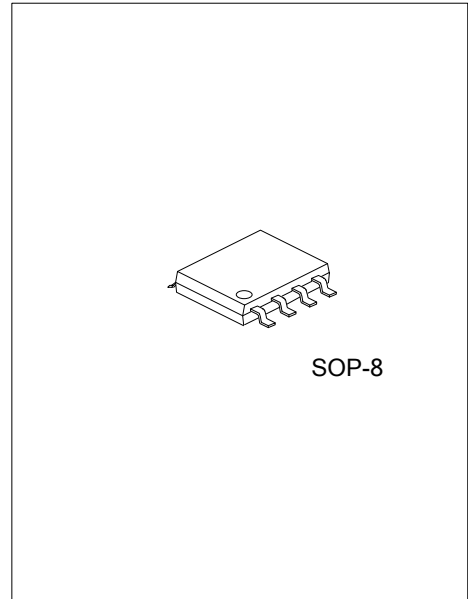
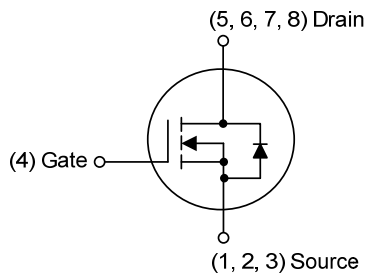
The UTC **UF7464** is a N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with low $R_{DS(ON)}$ characteristic by high cell density trench technology.

The UTC **UF7464** is suitable for high efficiency synchronous rectification in SMPS, UPS, hard switched and high frequency circuits.

FEATURES

- * $R_{DS(ON)} \leq 0.2 \Omega @ V_{GS}=10V, I_D=1.5A$
- * High switching speed
- * 100% avalanche tested

SYMBOL



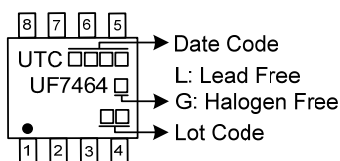
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UF7464L-S08-R	UF7464G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: S: Source G: Gate D: Drain

<p>UF7464G-S08-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) S08: SOP-8</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	200	V
Gate-Source Voltage		V_{GSS}	± 20	V
Continuous Drain Current	Continuous	I_D	3	A
Pulsed Drain Current	Pulsed (Note 2)	I_{DM}	12	A
Peak Diode Recovery dv/dt (Note 3)		dv/dt	4.3	V/nS
Power Dissipation		P_D	8.0	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $I_{SD} \leq 1.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J = 25^\circ\text{C}$.

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	90	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	15.6	$^\circ\text{C}/\text{W}$

Note: The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

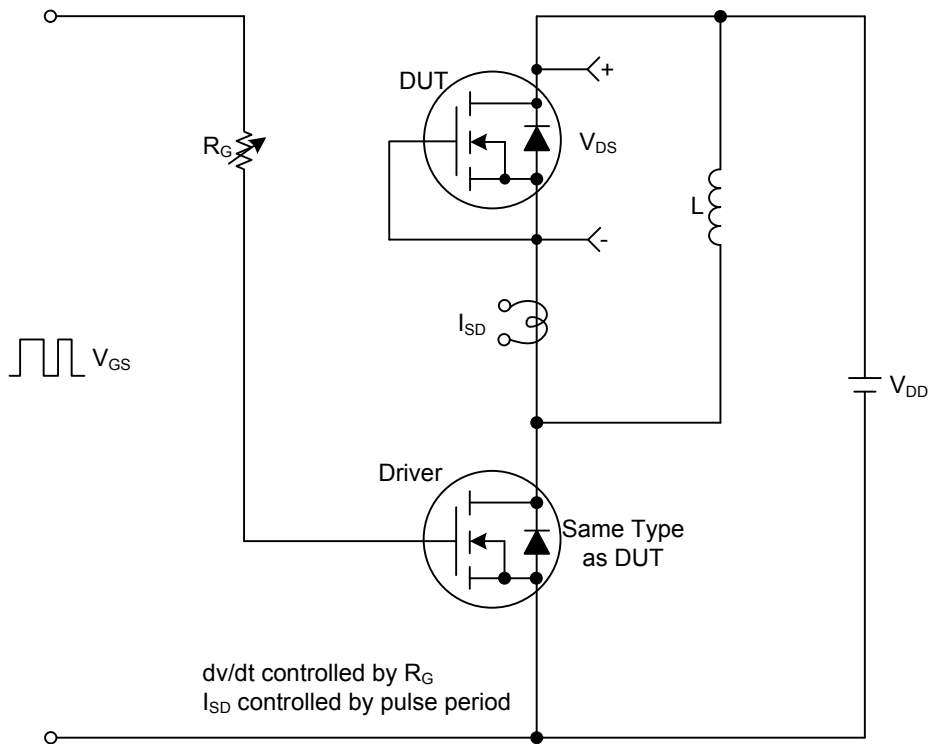
■ ELECTRICAL CHARACTERISTICS

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
OFF CHARACTERISTICS								
Drain-Source Breakdown Voltage		BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	200			V	
Drain-Source Leakage Current		I_{DSS}	$V_{DS}=160\text{V}$, $V_{GS}=0\text{V}$			10	μA	
Gate-Source Leakage Current	Forward	I_{GSS}	$V_{GS}=+20\text{V}$, $V_{DS}=0\text{V}$			100	nA	
	Reverse		$V_{GS}=-20\text{V}$, $V_{DS}=0\text{V}$			-100	nA	
ON CHARACTERISTICS								
Gate Threshold Voltage		$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V	
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=1.5\text{A}$			0.2	Ω	
DYNAMIC PARAMETERS								
Input Capacitance		C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1\text{MHz}$		1520		pF	
Output Capacitance		C_{OSS}				155		pF
Reverse Transfer Capacitance		C_{RSS}				13		pF
SWITCHING PARAMETERS								
Total Gate Charge (Note 1)		Q_G	$V_{DS}=160\text{V}$, $V_{GS}=10\text{V}$, $I_D=3\text{A}$ $I_G=1\text{mA}$ (Note 1, 2)		34		nC	
Gate to Source Charge		Q_{GS}				8		nC
Gate to Drain Charge		Q_{GD}				5		nC
Turn-on Delay Time (Note 1)		$t_{D(ON)}$	$V_{DD}=100\text{V}$, $V_{GS}=10\text{V}$, $I_D=3\text{A}$ $R_G=25\Omega$ (Note 1, 2)		12		ns	
Rise Time		t_R				18		ns
Turn-off Delay Time		$t_{D(OFF)}$				105		ns
Fall-Time		t_F				28		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS								
Maximum Body-Diode Continuous Current		I_S				3	A	
Maximum Body-Diode Pulsed Current		I_{SM}				12	A	
Drain-Source Diode Forward Voltage (Note 1)		V_{SD}	$I_S=3.0\text{A}$			1.3	V	
Reverse Recovery Time (Note 1)		t_{rr}	$I_S=3.0\text{A}$, $V_{GS}=0\text{V}$,			80	nS	
Reverse Recovery Charge		Q_{rr}	$di_f/dt=100\text{A}/\mu\text{s}$			420	nC	

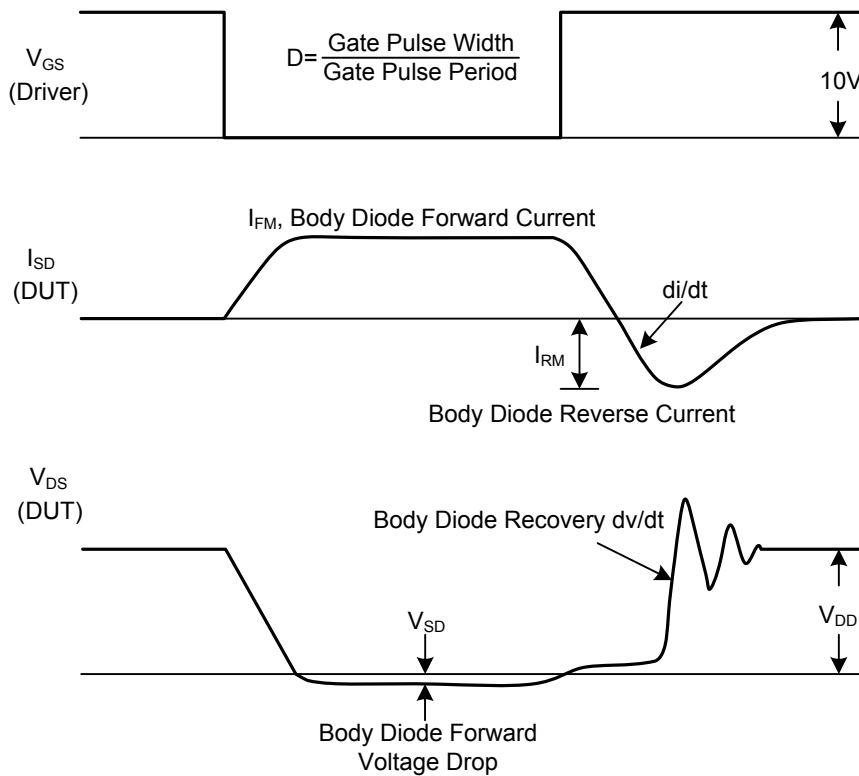
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

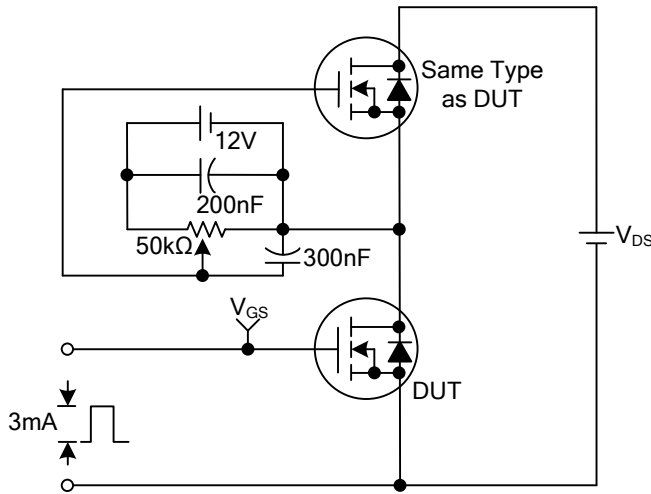
■ TEST CIRCUITS AND WAVEFORMS



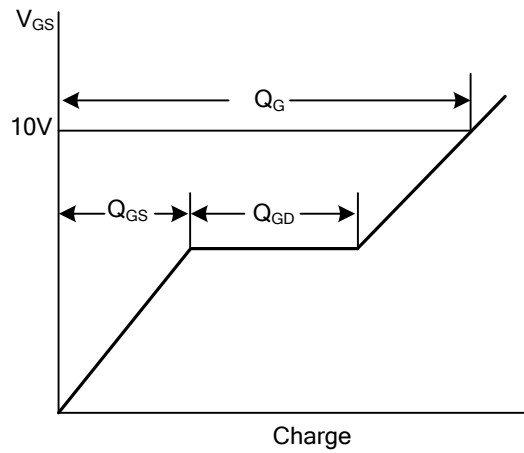
Peak Diode Recovery dv/dt Test Circuit & Waveforms



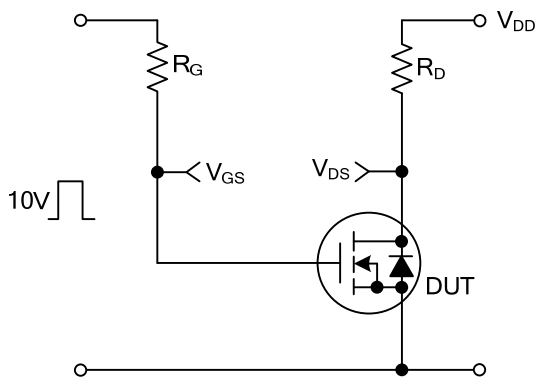
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



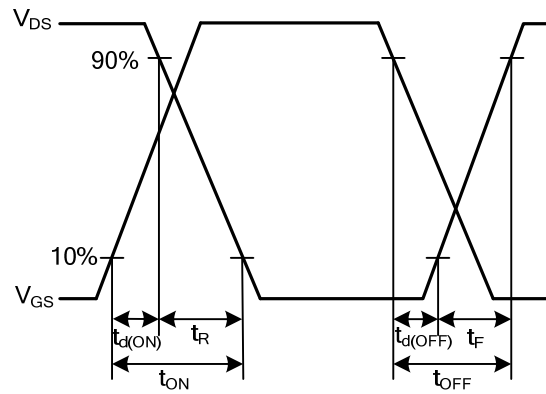
Gate Charge Test Circuit



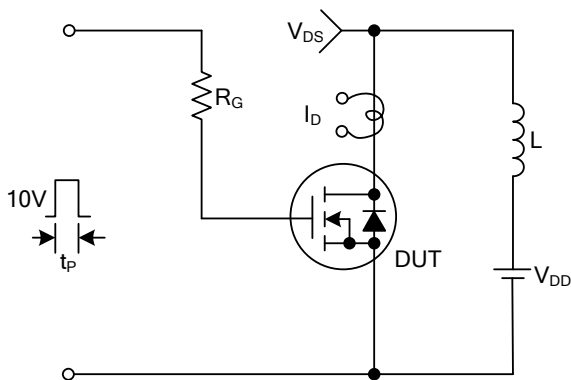
Gate Charge Waveforms



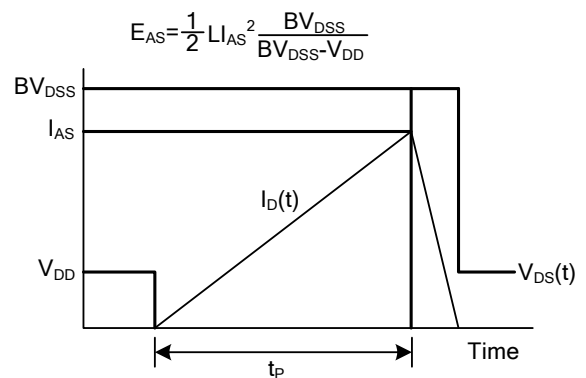
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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