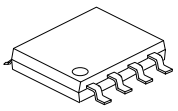
UF7464

Power MOSFET

3A, 200V N-CHANNEL ENHANCEMENT MODE TRENCH POWER MOSFET



SOP-8

■ DESCRIPTION

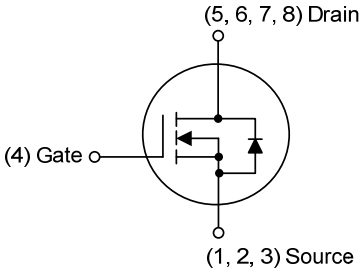
The UTC **UF7464** is a N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with low $R_{DS(ON)}$ characteristic by high cell density trench technology.

The UTC **UF7464** is suitable for high efficiency synchronous rectification in SMPS, UPS, hard switched and high frequency circuits.

■ FEATURES

* $R_{DS(ON)} \leq 0.2\ \Omega$ @ V_{GS}=10V, I_D=1.5A
* High switching speed
* 100% avalanche tested

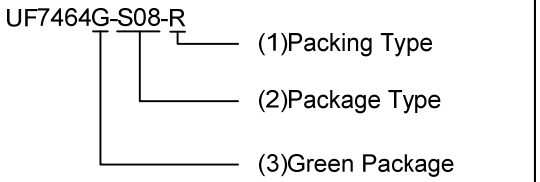
■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UF7464L-S08-R	UF7464G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: S: Source G: Gate D: Drain

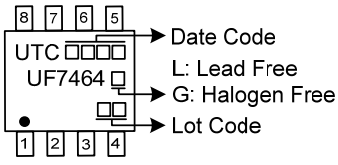


(1) R: Tape Reel

(2) S08: SOP-8

(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	200	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current	Continuous	I_D	3	A
Pulsed Drain Current	Pulsed (Note 2)	I_{DM}	12	A
Peak Diode Recovery dv/dt (Note 3)		dv/dt	4.3	V/nS
Power Dissipation		P_D	8.0	W
Junction Temperature		T_J	+150	°C
Storage Temperature Range		T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature.
3. I_{SD} ≤1.0A, di/dt ≤ 200A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J = 25°C.

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	90	°C/W
Junction to Case	θ_{JC}	15.6	°C/W

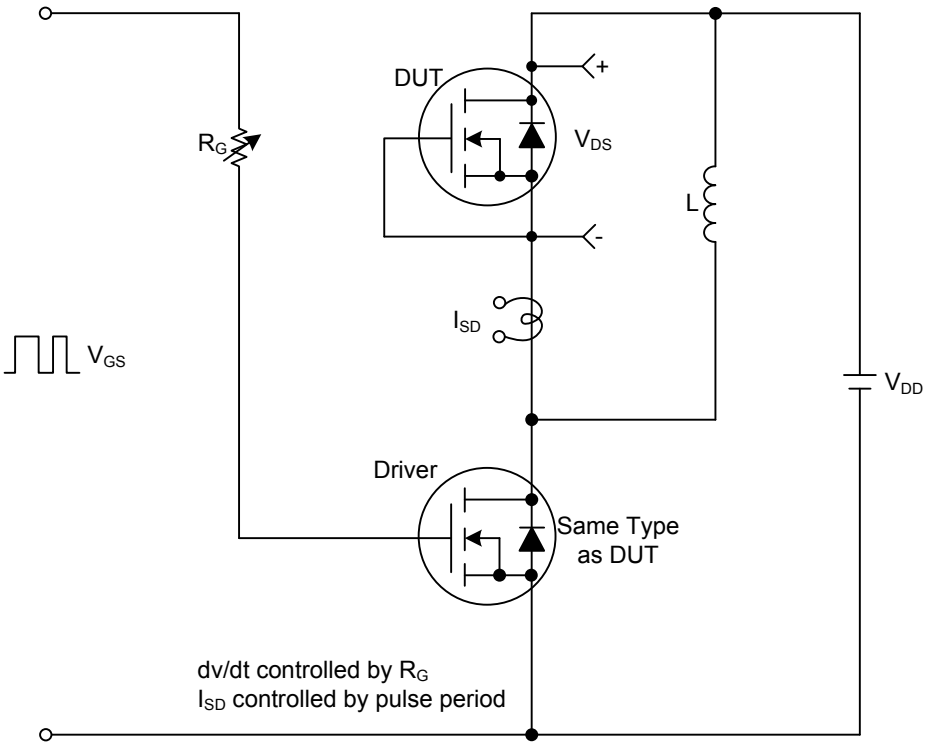
Note: The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

■ ELECTRICAL CHARACTERISTICS

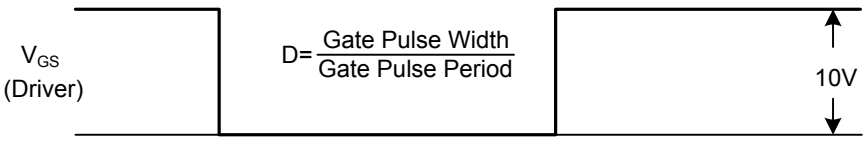
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	I_D=250μA, V_{GS}=0V	200			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=160V, V_{GS}=0V			10	μA
Gate-Source Leakage Current	Forward	I_{GSS}	V_{GS}=+20V, V_{DS}=0V			100	nA
	Reverse		V_{GS}=-20V, V_{DS}=0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=1.5A			0.2	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	V_{GS}=0V, V_{DS}=25V, f=1MHz		1520		pF
Output Capacitance		C_{OSS}			155		pF
Reverse Transfer Capacitance		C_{RSS}			13		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q_G	V_{DS}=160V, V_{GS}=10V, I_D=3A I_G=1mA (Note 1, 2)		34		nC
Gate to Source Charge		Q_{GS}			8		nC
Gate to Drain Charge		Q_{GD}			5		nC
Turn-on Delay Time (Note 1)		$t_{D(ON)}$	V_{DD}=100V, V_{GS}=10V, I_D=3A R_G=25Ω (Note 1, 2)		12		ns
Rise Time		t_R			18		ns
Turn-off Delay Time		$t_{D(OFF)}$			105		ns
Fall-Time		t_F			28		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				3	A
Maximum Body-Diode Pulsed Current		I_{SM}				12	A
Drain-Source Diode Forward Voltage (Note 1)		V_{SD}	I_S=3.0A			1.3	V
Reverse Recovery Time (Note 1)		t_{rr}	I_S=3.0A, V_{GS}=0V, dI_F/dt=100A/μs		80		nS
Reverse Recovery Charge		Q_{rr}			420		nC

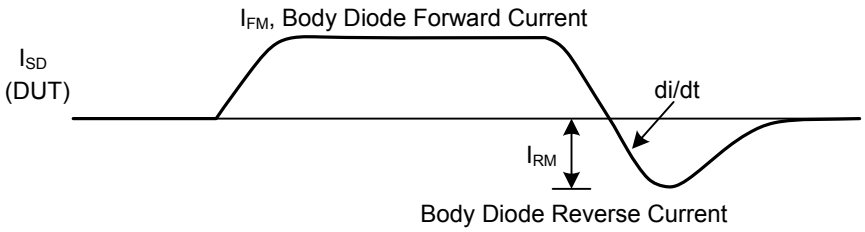
Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature.

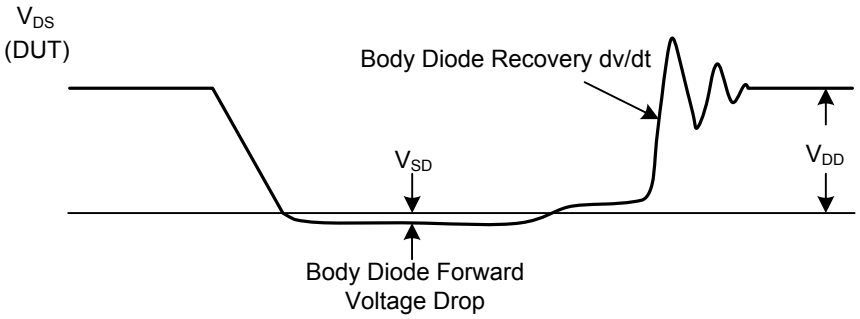
■ TEST CIRCUITS AND WAVEFORMS



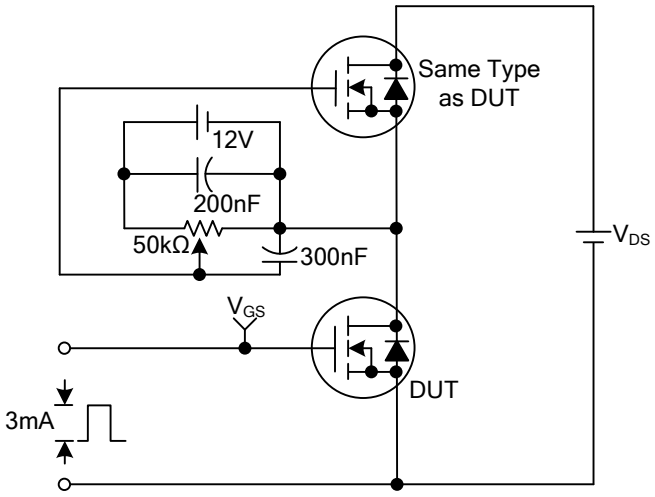
Peak Diode Recovery dv/dt Test Circuit & Waveforms



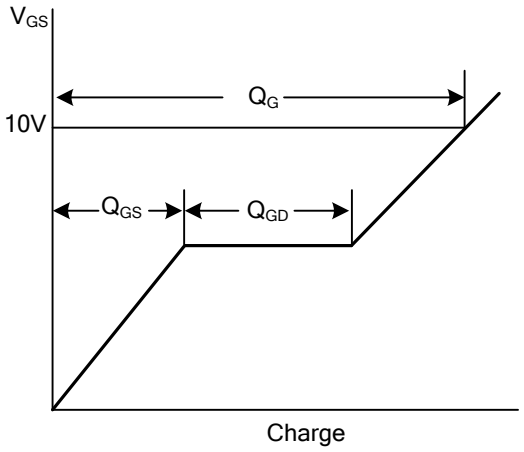




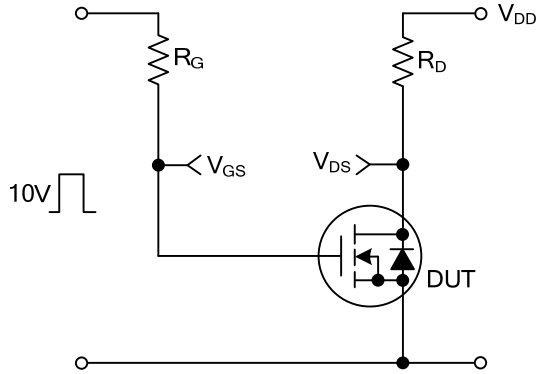
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



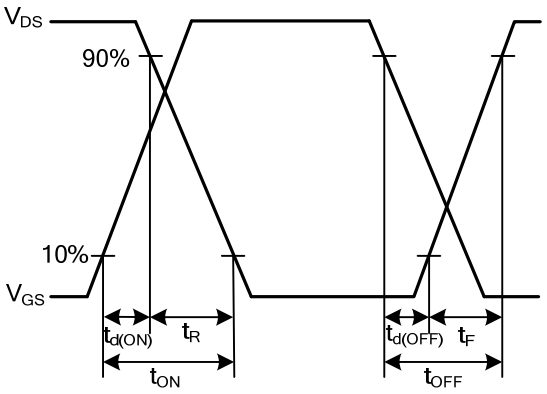
Gate Charge Test Circuit



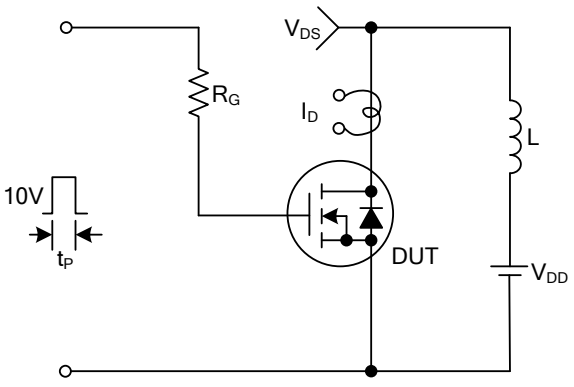
Gate Charge Waveforms



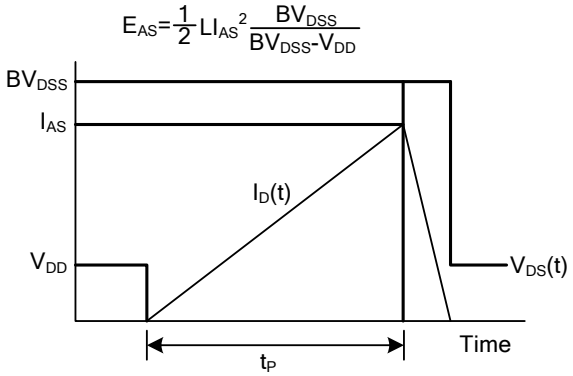
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms