



UF840-C

Preliminary

Power MOSFET

8.0A, 500V N-CHANNEL POWER MOSFET

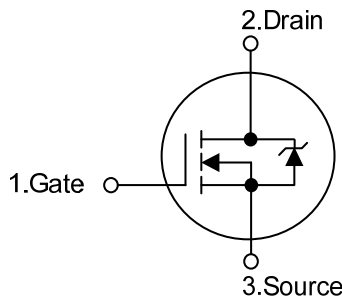
DESCRIPTION

The UTC **UF840-C** is a N-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications such as switching regulators, switching converters, solenoid, motor drivers, relay drivers.

FEATURES

- * Low $R_{DS(ON)} < 0.81\Omega @ V_{GS}=10V, I_D = 4.0A$
- * Single Pulse Avalanche Energy Rated
- * Fast Switching Speeds
- * Linear Transfer Characteristics
- * High Input Impedance

SYMBOL

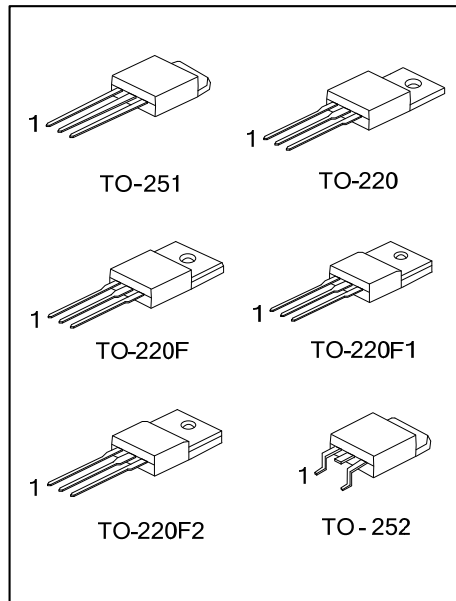


ORDERING INFORMATION

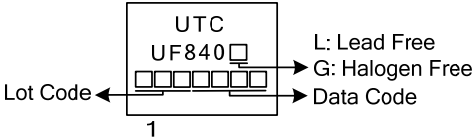
Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UF840L-TA3-T	UF840G-TA3-T	TO-220	G	D	S	Tube
UF840L-TF1-T	UF840G-TF1-T	TO-220F1	G	D	S	Tube
UF840L-TF3-T	UF840G-TF3-T	TO-220F2	G	D	S	Tube
UF840L-TF3-T	UF840G-TF3-T	TO-220F	G	D	S	Tube
UF840L-TM3-T	UF840G-TM3-T	TO-251	G	D	S	Tube
UF840L-TN3-R	UF840G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

	<p>(1) T: Tube, R: Tape Reel</p> <p>(2) TA3: TO-220, TF3: TO-220F, TF1: TO-220F1, TF2: TO-220F2, TM3: TO-251, TN3: TO-252</p> <p>(3) L: Lead Free, G: Halogen Free and Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless Otherwise Specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain to Source Voltage ($T_J = 25^\circ\text{C} \sim 125^\circ\text{C}$)		V_{DSS}	500	V
Gate to Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	8.0	A
	Pulsed (Note 2)	I_{DM}	32	A
Avalanche Current (Note 2)		I_{AR}	7.3	A
Single Pulse Avalanche Energy (Note 3)		E_{AS}	266	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	3.6	V/ns
Power Dissipation	TO-220	P_D	134	W
	TO-220F/TO-220F1		44	W
	TO-220F2		46	W
	TO-251/TO-252		123	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 10\text{mH}$, $I_{AS} = 7.3\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.

4. $I_{SD} \leq 8\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$.

■ THERMAL DATA

PARAMETER	PACKAGE	SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220/TO-220F	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
	TO-220F1/TO-220F2			
	TO-251/TO-252			
Junction to Case	TO-220	θ_{JC}	0.93	$^\circ\text{C}/\text{W}$
	TO-220F/TO-220F1		2.86	$^\circ\text{C}/\text{W}$
	TO-220F2		2.72	$^\circ\text{C}/\text{W}$
	TO-251/TO-252		1.01	$^\circ\text{C}/\text{W}$

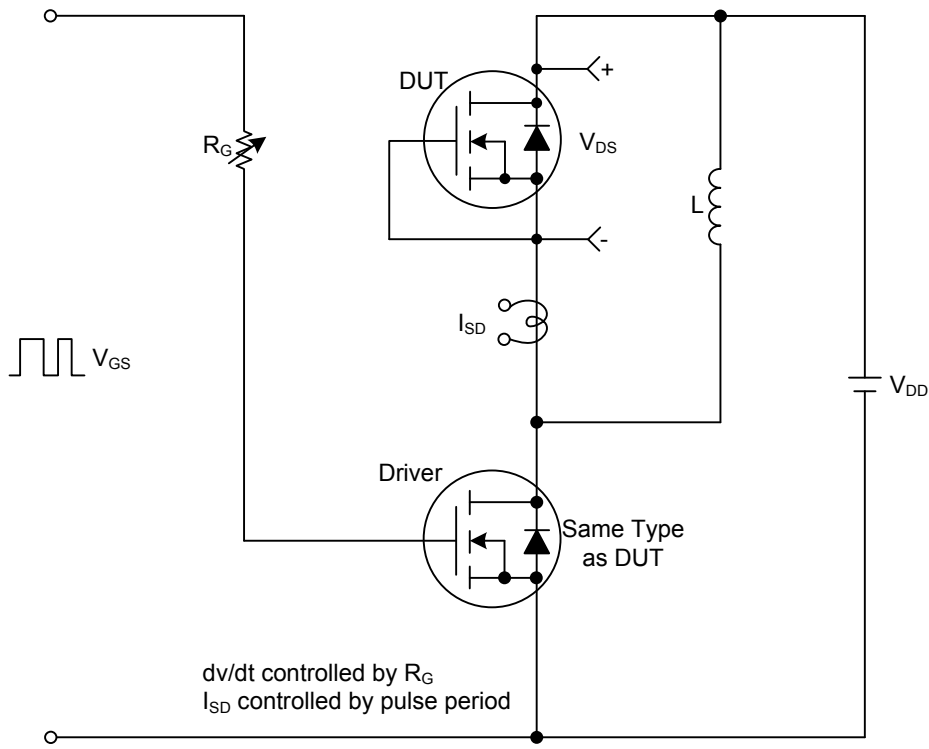
■ ELECTRICAL SPECIFICATIONS (T_J=25°C, unless Otherwise Specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V	500			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =550V, V _{GS} =0V			25	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} = ±30V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} =V _{DS} , I _D = 250μA	2.0		4.0	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =4.0A			0.81	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		1120		pF
Output Capacitance	C _{OSS}			120		pF
Reverse Transfer Capacitance	C _{RSS}			10		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q _G	V _{DS} =50V, V _{GS} =10V, I _D =1.3A I _G =100μA (Note 1, 2)		78		nC
Gate to Source Charge	Q _{GD}			6		nC
Gate to Drain Charge	Q _{GS}			11.5		nC
Turn-ON Delay Time (Note 1)	t _{D(ON)}	V _{DD} =30V, V _{GS} =10V, I _D =0.5A, R _G =25Ω (Note 1, 2)		60		ns
Rise Time	t _R			57		ns
Turn-OFF Delay Time	t _{D(OFF)}			274		ns
Fall-Time	t _F			69		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I _S				8	A
Maximum Body-Diode Pulsed Current	I _{SM}				32	A
Drain-Source Diode Forward Voltage (Note 1)	V _{SD}	I _S =8.0A, V _{GS} =0V			2	V
Body Diode Reverse Recovery Time (Note 1)	t _{rr}	I _S =8.0A, V _{GS} =0V, dI _F /dt=100A/μs		330		ns
Body Diode Reverse Recovery Charge	Q _{rr}				2.6	

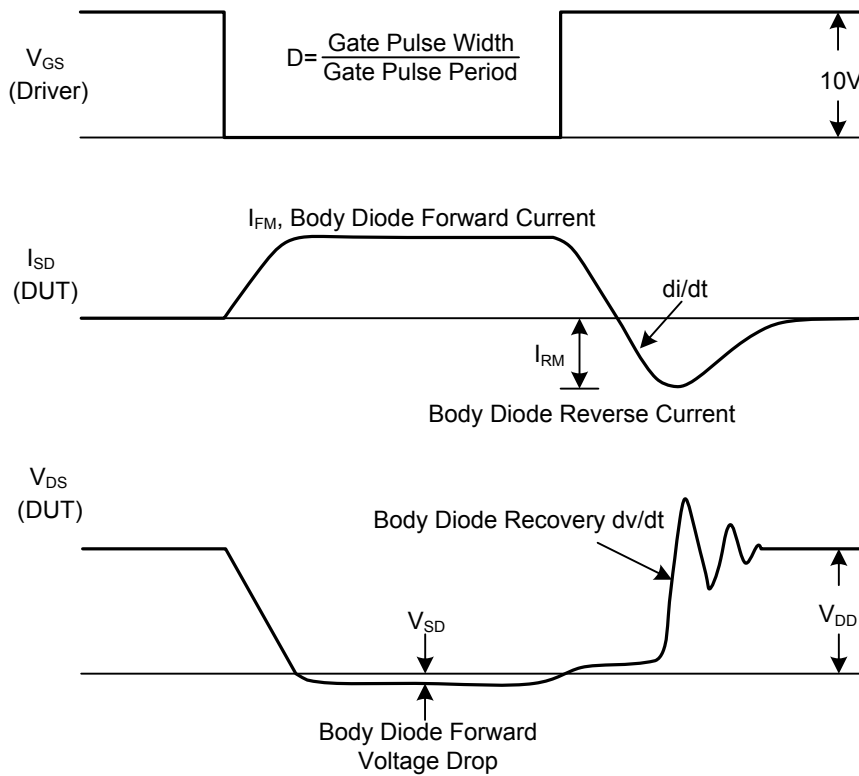
Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

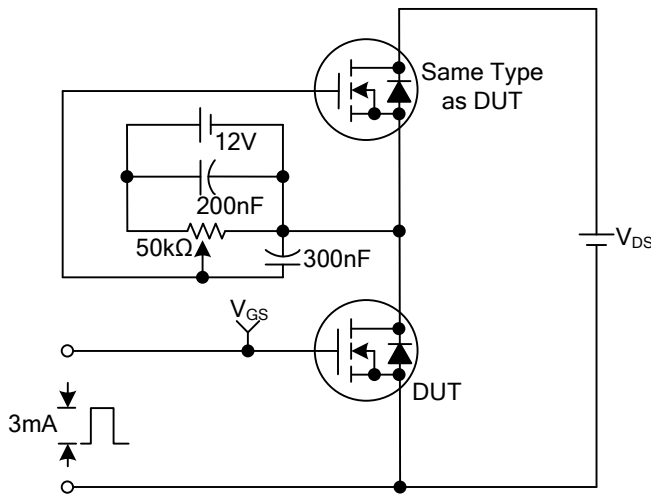


Peak Diode Recovery dv/dt Test Circuit & Waveforms

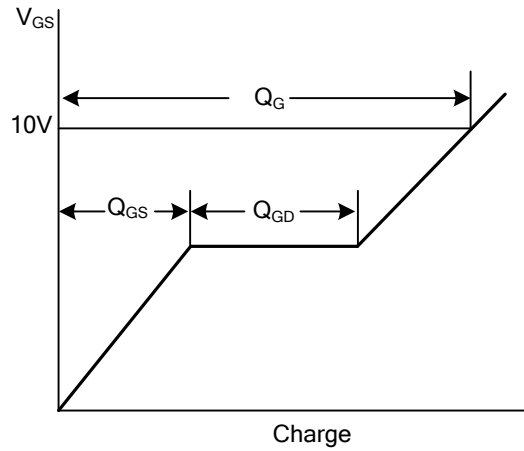


Peak Diode Recovery dv/dt Waveforms

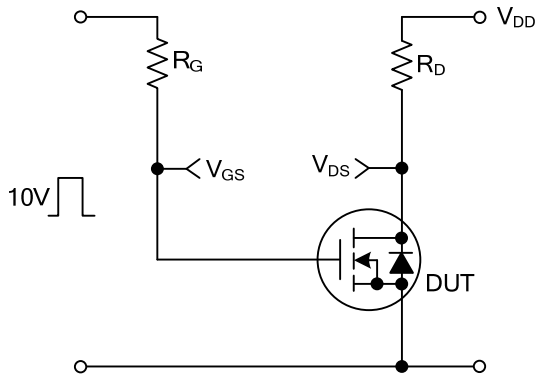
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



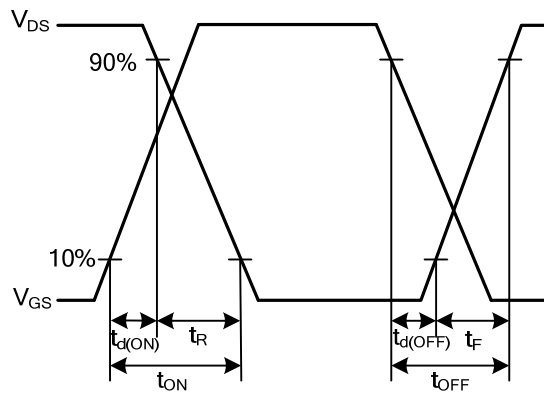
Gate Charge Test Circuit



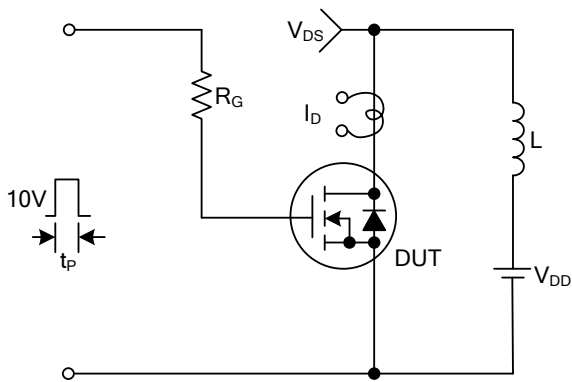
Gate Charge Waveforms



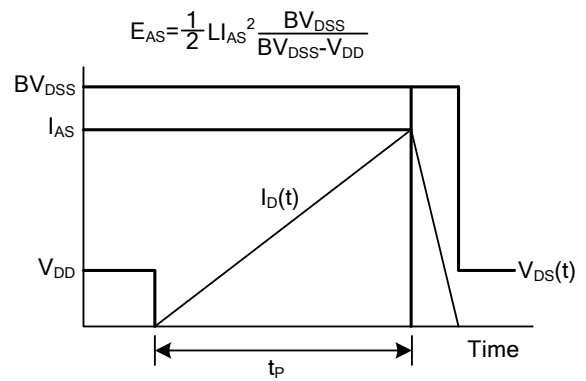
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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