



3NM50

Preliminary

Power MOSFET

3.0A, 500V N-CHANNEL SUPER-JUNCTION MOSFET

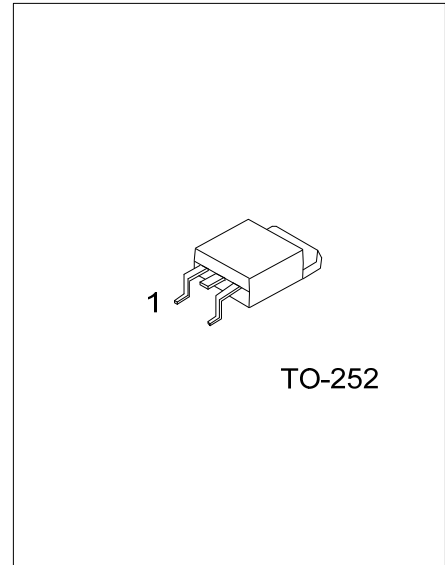
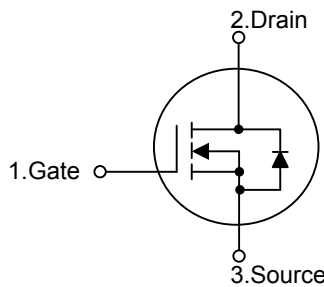
■ DESCRIPTION

The **UTC 3NM50** is a Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and a high rugged avalanche characteristics. This power MOSFET is usually used at DC-DC, AC-DC converters for power applications.

■ FEATURES

- * $R_{DS(ON)} < 1.8\Omega @ V_{GS}=10V, I_D=1.5A$
- * High Switching Speed
- * 100% Avalanche Tested

■ SYMBOL



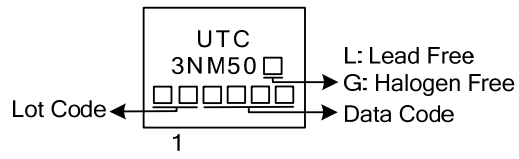
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
3NM50L-TN3-R	3NM50G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>3NM50L-TN3-R</p>	<p>(1) R: Tape Reel</p> <p>(2) TN3: TO-252</p> <p>(3) L: Lead Free, G: Halogen Free and Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current ($T_C=25^\circ\text{C}$)	Continuous	I_D	3.0	A
	Pulsed (Note 2)	I_{DM}	12	A
Avalanche Current (Note 2)		I_{AR}	2.4	A
Avalanche Energy (Note 3)	Single Pulsed	E_{AS}	29	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	5.3	V/ns
Power Dissipation		P_D	50	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

- Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
 2. Repetitive Rating: Pulse width limited by maximum junction temperature.
 3. $L=10\text{mH}$, $I_{AS}=2.4\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\ \Omega$, Starting $T_J = 25^\circ\text{C}$.
 4. $I_{SD}\leq 3.0\text{A}$, $di/dt\leq 200\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$.

■ THERMAL DATA

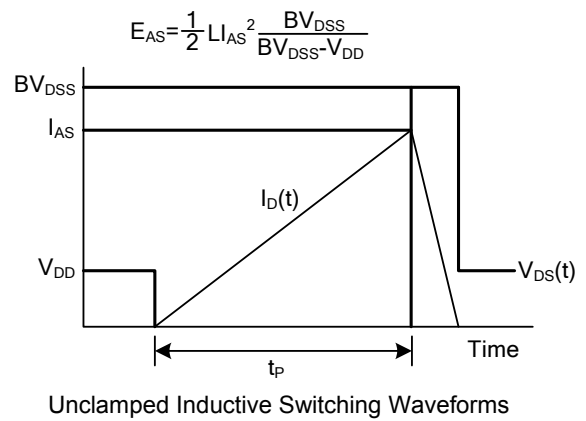
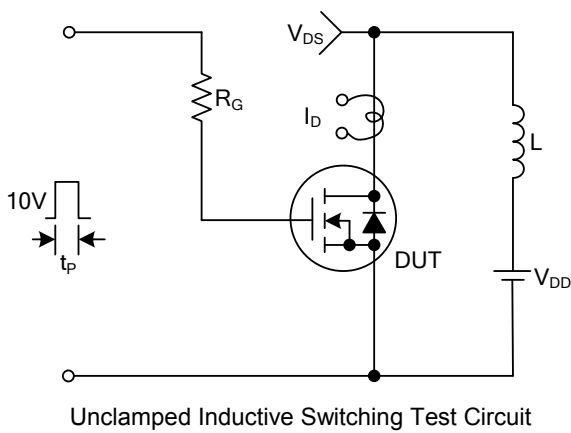
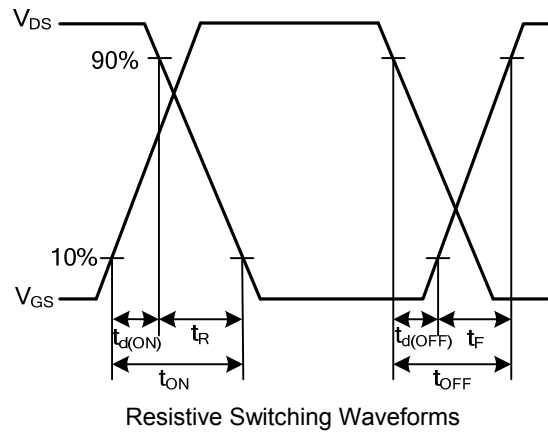
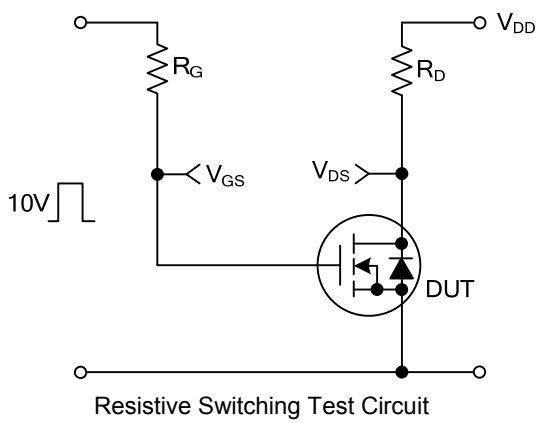
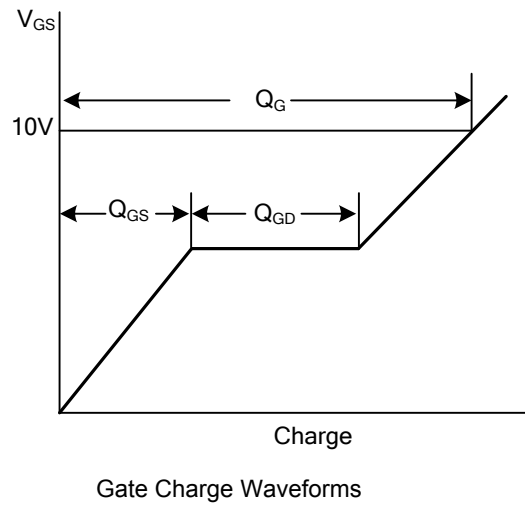
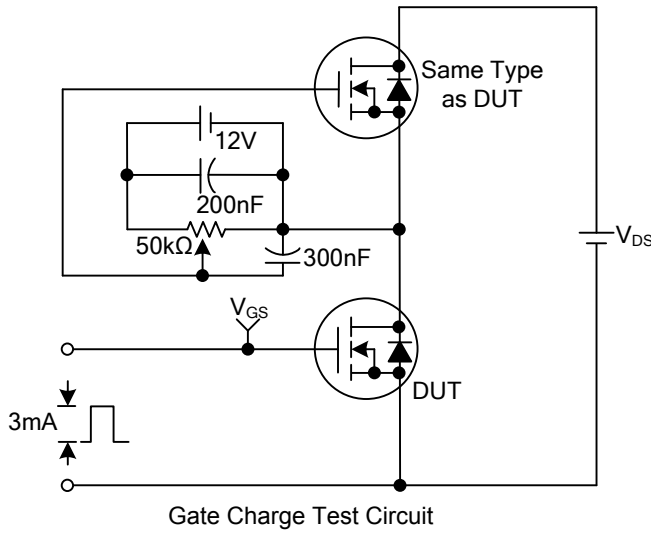
PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	110	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	2.5	$^\circ\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise noted)

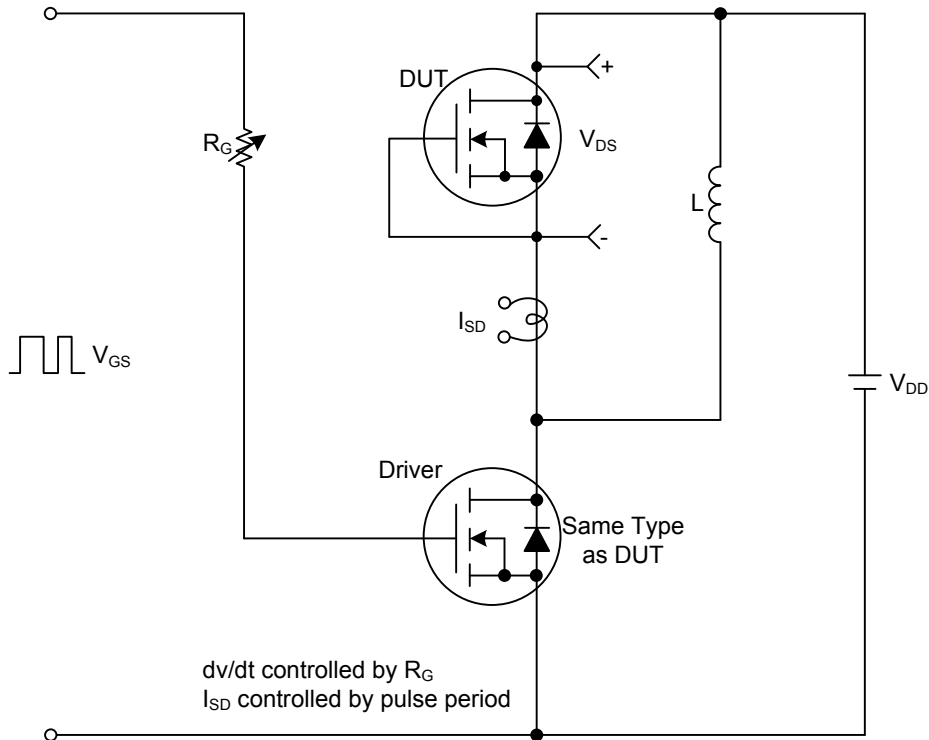
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	500			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=500\text{V}$, $V_{GS}=0\text{V}$			10	μA
Gate- Source Leakage Current	Forward	$V_{GS}=+30\text{V}$, $V_{DS}=0\text{V}$			+100	nA
	Reverse	$V_{GS}=-30\text{V}$, $V_{DS}=0\text{V}$			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.5		4.5	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=1.5\text{A}$			1.8	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		155		pF
Output Capacitance	C_{OSS}			137		pF
Reverse Transfer Capacitance	C_{RSS}			25		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q_G	$V_{DS}=50\text{V}$, $V_{GS}=10\text{V}$, $I_D=1.3\text{A}$, $I_G = 250\mu\text{A}$ (Note 1, 2)		35		nC
Gate to Source Charge	Q_{GS}			3		nC
Gate to Drain Charge	Q_{GD}			7.5		nC
Turn-ON Delay Time (Note 1)	$t_{D(ON)}$	$V_{DD} = 30\text{V}$, $V_{GS}=10\text{V}$, $I_D = 0.5\text{A}$, $R_G=25\ \Omega$ (Note 1, 2)		37		ns
Rise Time	t_R			37		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			82		ns
Fall-Time	t_F			44		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				3	A
Maximum Body-Diode Pulsed Current	I_{SM}				12	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S=3.0\text{A}$, $V_{GS}=0\text{V}$			1.4	V
Reverse Recovery Time (Note 1)	t_{rr}	$I_S=3.0\text{A}$, $V_{GS}=0\text{V}$,		210		ns
Reverse Recovery Charge	Q_{rr}	$di/dt = 100\text{A}/\mu\text{s}$		1.2		μC

- Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.
 2. Essentially independent of operating temperature.

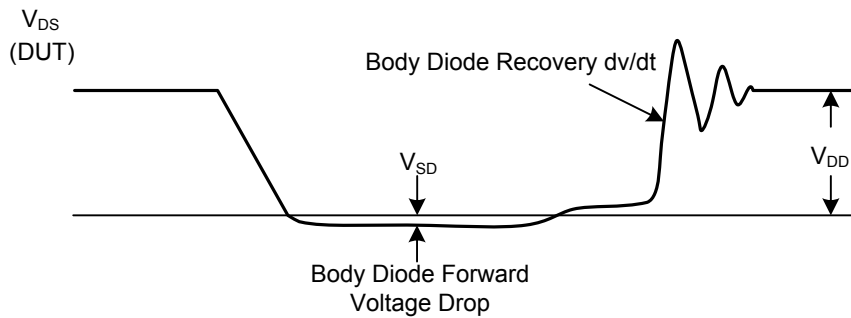
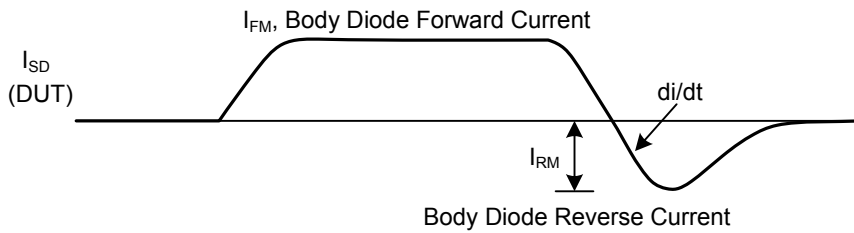
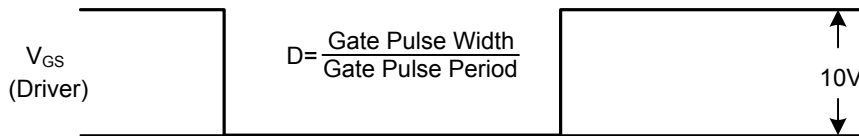
■ TEST CIRCUITS AND WAVEFORMS



■ TEST CIRCUITS AND WAVEFORMS(Cont.)



Peak Diode Recovery dv/dt Test Circuit & Waveforms



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