



7NM50

Preliminary

Power MOSFET

7.0A, 500V N-CHANNEL SUPER-JUNCTION MOSFET

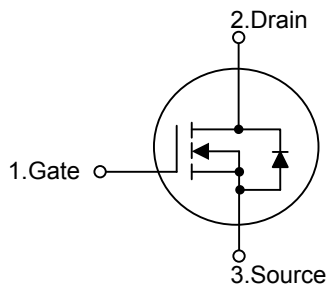
DESCRIPTION

The **UTC 7NM50** is a Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and a high rugged avalanche characteristics. This power MOSFET is usually used at DC-DC, AC-DC converters for power applications.

FEATURES

- * $R_{DS(ON)} < 0.55\Omega @ V_{GS}=10V, I_D=3.5A$
- * High Switching Speed
- * 100% Avalanche Tested

SYMBOL



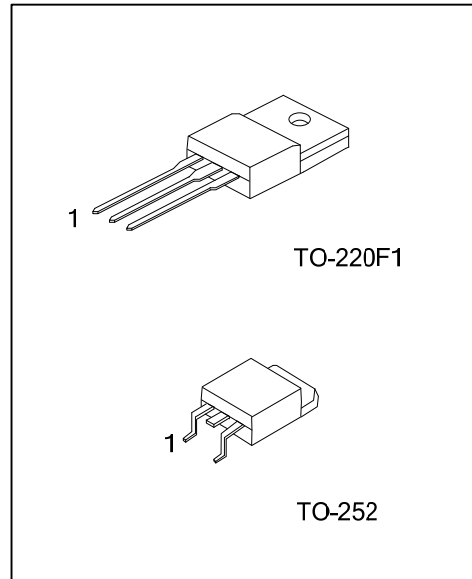
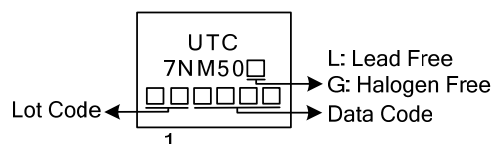
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
7NM50L-TF1-T	7NM50G-TF1-T	TO-220F1	G	D	S	Tube
7NM50L-TN3-R	7NM50G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>7NM50G-TF1-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) T: Tube, R: Tape Reel</p> <p>(2) TF1: TO-220F1, TN3: TO-252</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	7.0	A
	Pulsed (Note 2)	I_{DM}	28	A
Avalanche Current (Note 2)		I_{AR}	2.1	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	101	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	7.58	V/ns
Power Dissipation	TO-220F1	P_D	40	W
	TO-252		60	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 46\text{mH}$, $I_{AS} = 2.1\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 7.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220F1	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
	TO-252		110	$^\circ\text{C}/\text{W}$
Junction to Case	TO-220F1	θ_{JC}	3.1	$^\circ\text{C}/\text{W}$
	TO-252		2.08	$^\circ\text{C}/\text{W}$

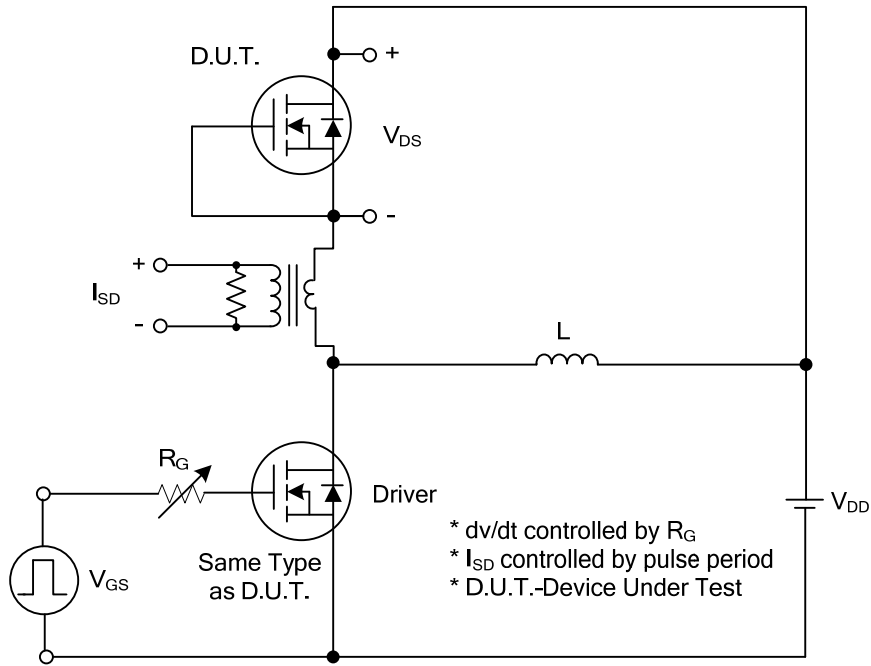
■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	500			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=500\text{V}$, $V_{GS}=0\text{V}$			1	μA
Gate- Source Leakage Current	Forward	I_{GSS}			+100	nA
	Reverse				-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.5		4.5	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=3.5\text{A}$			0.55	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		530		pF
Output Capacitance	C_{OSS}			425		pF
Reverse Transfer Capacitance	C_{RSS}			40		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q_G	$V_{DS}=50\text{V}$, $I_D=1.3\text{A}$, $I_G=100\mu\text{A}$ $V_{GS}=10\text{V}$ (Note 1,2)		50		nC
Gate to Source Charge	Q_{GS}			5		nC
Gate to Drain Charge	Q_{GD}			14		nC
Turn-ON Delay Time (Note 1)	$t_{D(ON)}$	$V_{DD}=30\text{V}$, $I_D=0.5\text{A}$, $R_G=25\Omega$, $V_{GS}=10\text{V}$ (Note 1,2)		50		ns
Rise Time	t_R			100		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			170		ns
Fall-Time	t_F			78		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				7	A
Maximum Body-Diode Pulsed Current	I_{SM}				28	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S=7\text{A}$, $V_{GS}=0\text{V}$			1.4	V
Body Diode Reverse Recovery Time (Note 1)	t_{rr}	$I_S=7\text{A}$, $V_{GS}=0\text{V}$, $dI_F/dt=100\text{A}/\mu\text{s}$ (Note 1)		315		ns
Body Diode Reverse Recovery Charge	Q_{rr}				3	

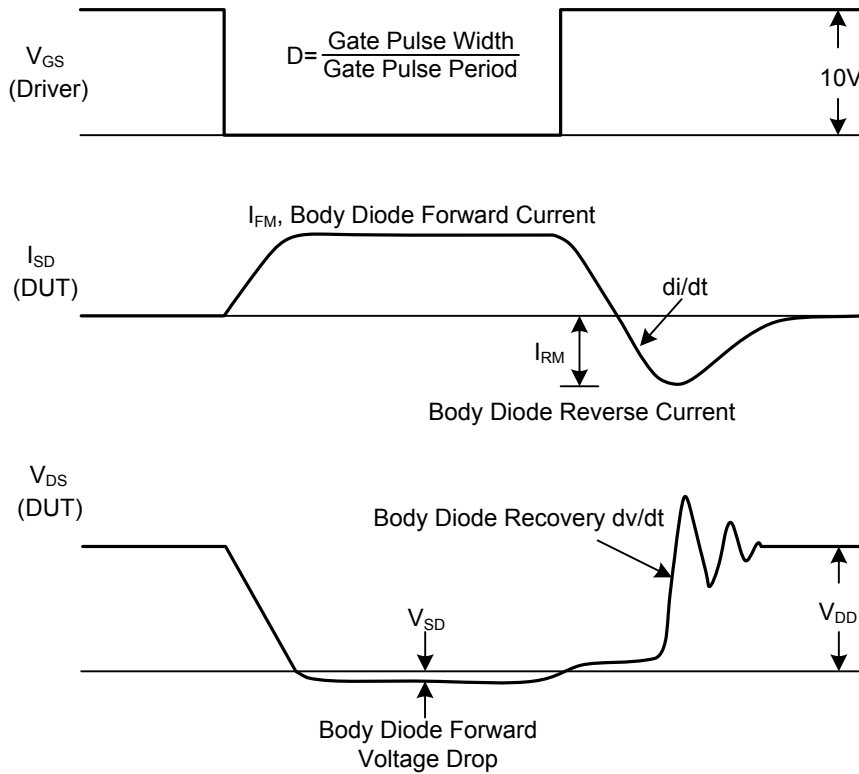
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

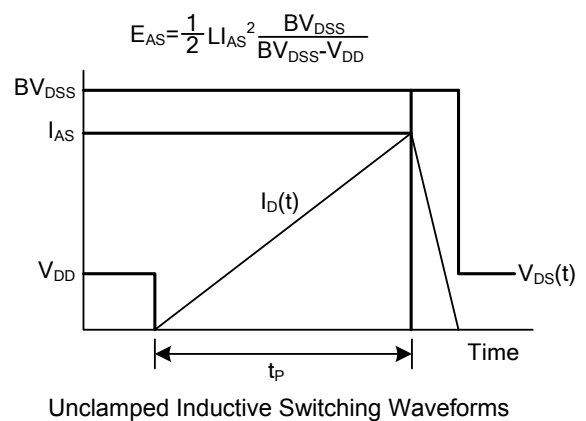
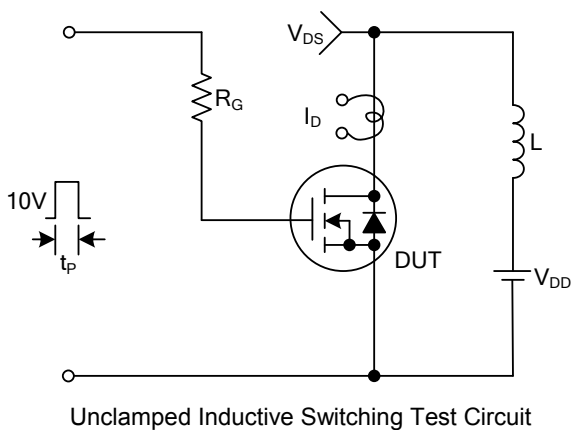
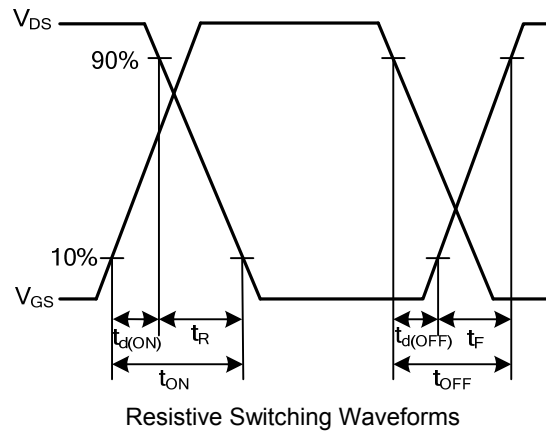
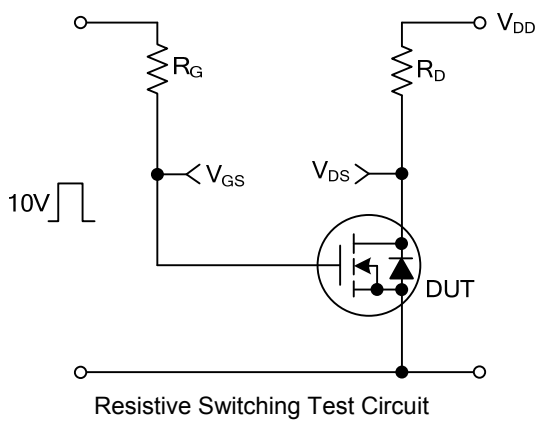
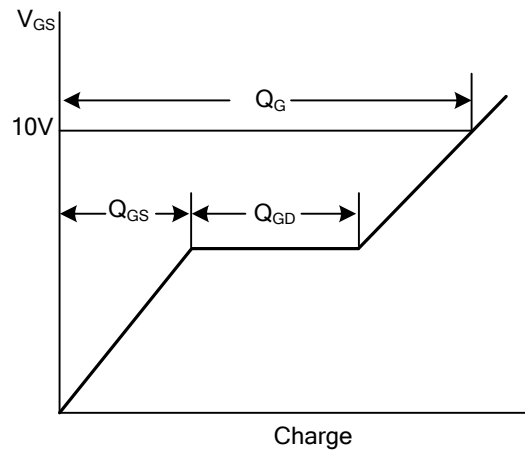
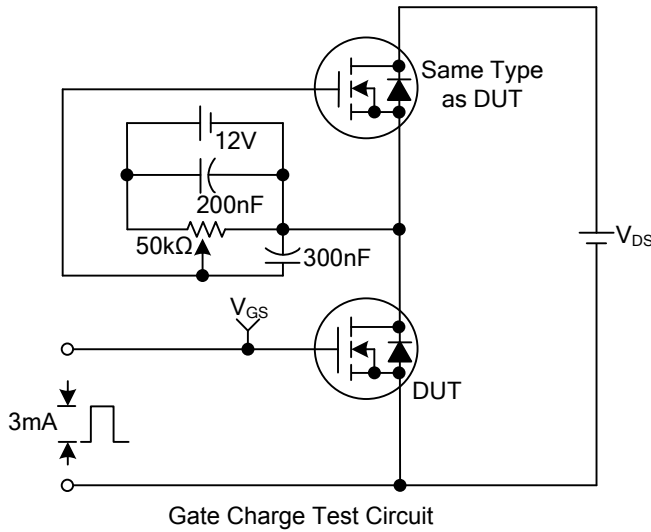


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)



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