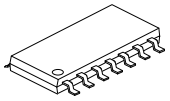
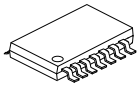
U74HC73

CMOS IC

DUAL J-K FLIP-FLOPS WITH CLEAR AND PRESET



SOP-14



TSSOP-14

■ DESCRIPTION

The **U74HC73** is a dual J-K negative-edge-triggered flip-flop.

The clear ($\overline{CLR}$) input can reset the output at a low level, regardless of the level of others inputs. when the $\overline{CLR}$ is inactive(high), data at the data inputs meeting the set-up time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Following the hold-time interval, data J and k inputs can be changed without affecting the levels at the outputs.

■ FEATURES

* Wide supply voltage range from 2.0V to 6.0V
* Low static power consumption; I_{CC}=4μA (Max.)

■ ORDERING INFORMATION

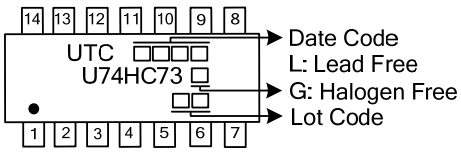
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC73L-S14-R	U74HC73G-S14-R	SOP-14	Tape Reel
U74HC73L-P14-R	U74HC73G-P14-R	TSSOP-14	Tape Reel

U74HC73G-S14-R

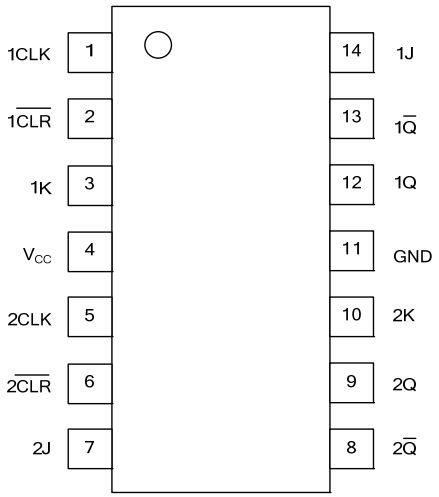
(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) S14: SOP-14, P14: TSSOP-14
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION

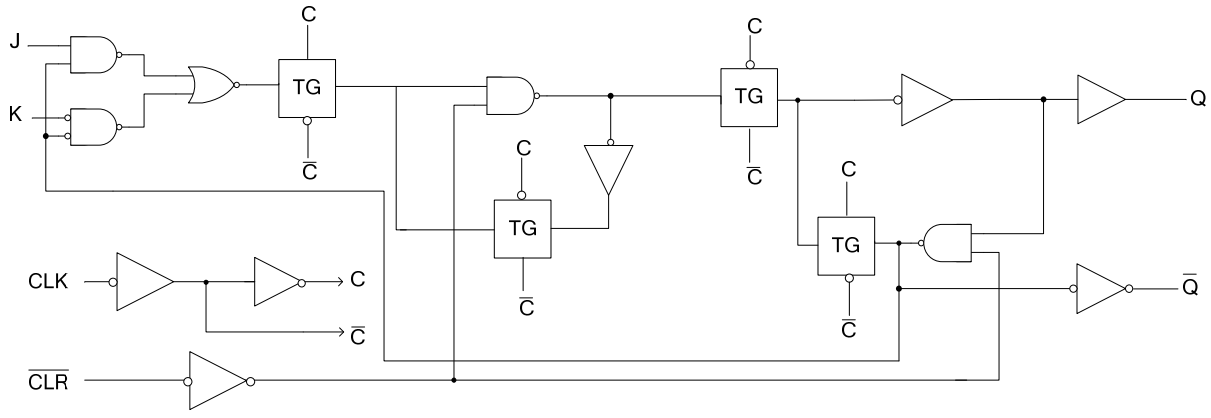


■ FUNCTION TABLE

INPUT				OUTPUT	
$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

Note: This configuration is unstable, as it is not persist when either $\overline{PRE}$ or $\overline{CLR}$ return to high level.

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (Note 2)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +7.0	V
Input Voltage	V_{IN}		-0.5 ~ V_{CC}+0.5	V
Output Voltage	V_{OUT}	Active Mode	-0.5 ~ V_{CC}+0.5	V
Continuous V_{CC} or GND Current	I_{CC}		±50	μA
Continuous Output Current	I_{OUT}	V_{OUT}=0V ~ V_{CC}	±25	mA
Input Clamp Current	I_{IK}	V_{IN}<0V or V_{IN}>V_{CC}	±20	mA
Output Clamp Current	I_{OK}	V_{OUT}>V_{CC} or V_{OUT}<0V	±20	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.0	5.0	6.0	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise or Fall Rate	Δt/Δv	V_{CC}=2.0V			1000	ns
		V_{CC}=4.5V			500	ns
		V_{CC}=6.0V			400	ns
Operating Temperature	T_A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
High-level Input Voltage	V_{IH}	V_{CC}=2.0V		1.5			V
		V_{CC}=4.5V		3.15			V
		V_{CC}=6.0V		4.2			V
Low-level Input Voltage	V_{IL}	V_{CC}=2.0V				0.5	V
		V_{CC}=4.5V				1.35	V
		V_{CC}=6.0V				1.8	V
High-Level Output Voltage	V_{OH}	V_{CC}=2.0V	V_{IN}=V_{IH} or V_{IL} I_{OH}=-20μA	1.9	1.998		V
		V_{CC}=4.5V		4.4	4.499		V
		V_{CC}=6.0V		5.9	5.999		V
		V_{CC}=4.5V, V_{IN}=V_{IH} or V_{IL} I_{OH}=-4mA		3.98	4.3		V
		V_{CC}=6.0V, V_{IN}=V_{IH} or V_{IL} I_{OH}=-5.2mA		5.48	5.8		V
Low-Level Output Voltage	V_{OL}	V_{CC}=2.0V	V_{IN}=V_{IH} or V_{IL} I_{OL}=20μA		0.002	0.1	V
		V_{CC}=4.5V			0.001	0.1	V
		V_{CC}=6.0V			0.001	0.1	V
		V_{CC}=4.5V, V_{IN}=V_{IH} or V_{IL}, I_{OL}=4mA			0.17	0.26	V
		V_{CC}=6.0V, V_{IN}=V_{IH} or V_{IL} I_{OL}=5.2mA			0.15	0.26	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=6.0V, V_{IN}= V_{CC} or GND				±0.1	μA
Quiescent Supply Current	I_{CC}	V_{CC}=6.0V, V_{IN}=V_{CC} or GND, I_{OUT}=0A				4	μA
Input Capacitance	C_I	V_{CC}=2.0~6.0V, V_{IN}=V_{CC} or GND			3	10	pF

■ SWITCHING CHARACTERISTICS (C_L=50pF, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum clock pulse frequency	f_{MAX}	V_{CC}=2.0V	6	11		MHz
		V_{CC}=4.5V	31	54		MHz
		V_{CC}=6.0V	36	64		MHz
Propagation delay from input ($\overline{CLR}$) to output (Q or $\overline{Q}$)	t_{PHL}	V_{CC}=2.0V		78	155	ns
		V_{CC}=4.5V		16	31	ns
		V_{CC}=6.0V		13	26	ns
Propagation delay from input (CLK) to output (Q or $\overline{Q}$)	t_{PD}	V_{CC}=2.0V		63	126	ns
		V_{CC}=4.5V		13	25	ns
		V_{CC}=6.0V		11	21	ns
Propagation delay to output (Any)	t_t	V_{CC}=2.0V		38	75	ns
		V_{CC}=4.5V		8	15	ns
		V_{CC}=6.0V		6	13	ns

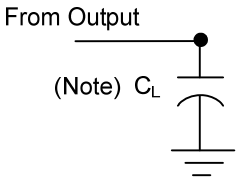
■ TIMING REQUIREMENTS (Input: t_R, t_F≤2.5ns; PRR≤1MHz, unless otherwise specified))

PARAMETER		SYMBOL	Conditions	MIN	TYP	MAX	UNIT
Clock frequency		f_{CLOCK}	V_{CC}= 2V			6	MHZ
			V_{CC}=4.5V			31	MHZ
			V_{CC}=6V			36	MHZ
Pulse duration	CLK High or Low	t_W	V_{CC}= 2V	80			ns
			V_{CC}=4.5V	16			ns
			V_{CC}=6V	14			ns
Pulse duration	$\overline{CLR}$ Low	t_W	V_{CC}= 2V	80			ns
			V_{CC}=4.5V	16			ns
			V_{CC}=6V	14			ns
Setup time before CLK↓		t_{SU}	V_{CC}= 2V	100			ns
			V_{CC}=4.5V	25			ns
			V_{CC}=6V	20			ns
Hold time ,data after CLK↓		t_H	V_{CC}= 2V	0			ns
			V_{CC}=4.5V	0			ns
			V_{CC}=6V	0			ns

■ OPERATING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No load.		30		pF

■ TEST CIRCUIT AND WAVEFORMS



Note: C_L includes probe and jig capacitance. C_L=50pF, R_L=1KΩ.

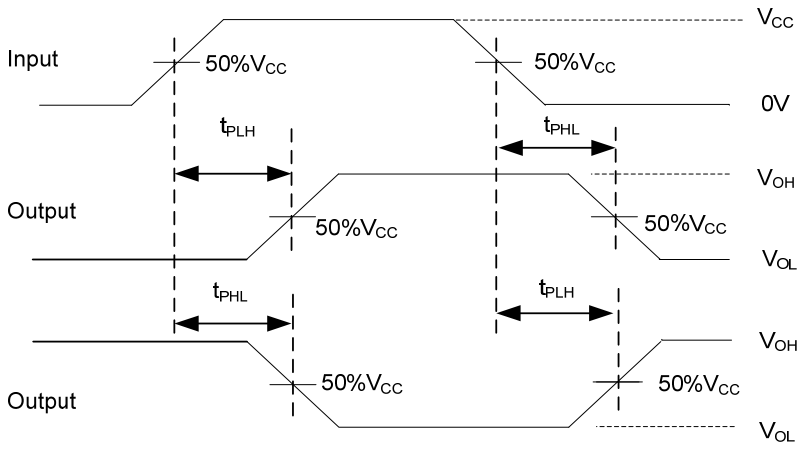


Fig 1. Load circuitry for switching times

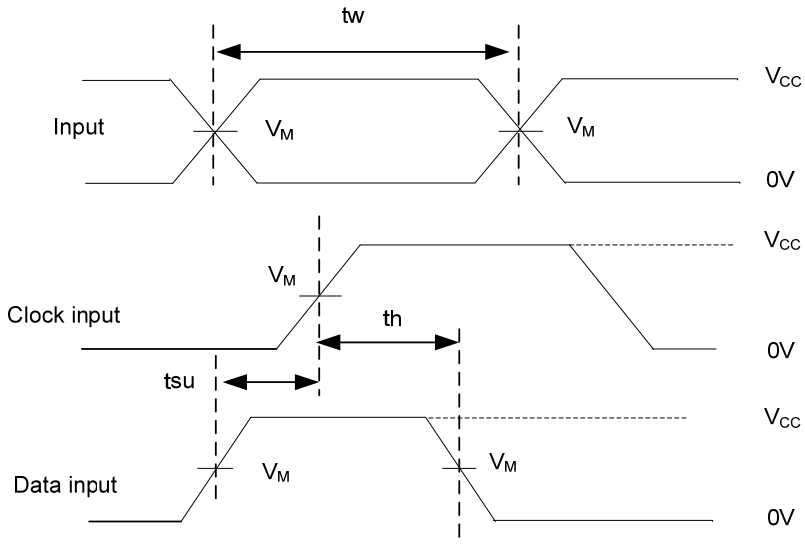


Fig 2. Propagation delay from input to output and input voltage waveforms.

Notes: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O = 50Ω.