



## U74LVC3G07

CMOS IC

### TRIPLE BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

#### DESCRIPTION

The **U74LVC3G07** is triple bus buffer/driver with open-drain outputs. The output can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

This device has power-down protective circuit, preventing device destruction when it is powered down.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### FEATURES

- \* Wide supply voltage range from 1.65V to 5.5V
- \* Inputs accept voltages up to 5.5V
- \*  $I_{OFF}$  supports partial-power-down mode
- \* Low static power consumption;  $I_{CC}=10\mu A$  (Max.)

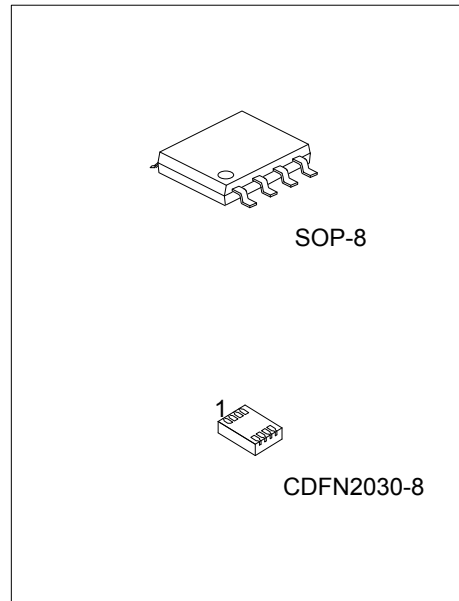
#### ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC3G07L-S08-R	U74LVC3G07G-S08-R	SOP-8	Tape Reel
U74LVC3G07L-CK08-2030-R	U74LVC3G07G-CK08-2030-R	CDFN2030-8	Tape Reel

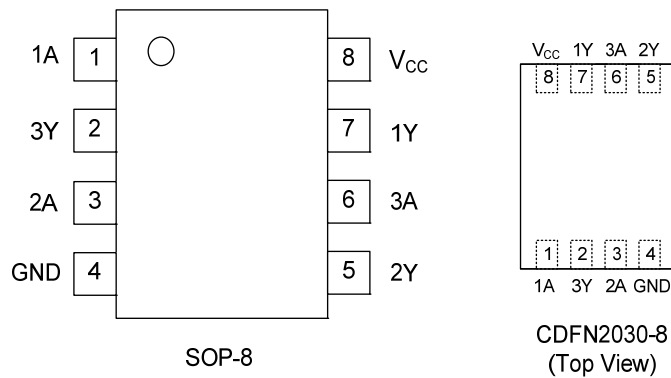
<p>U74LVC3G07G-S08-R</p> <ul style="list-style-type: none"> <li>(1) Packing Type</li> <li>(2) Package Type</li> <li>(3) Green Package</li> </ul>	<ul style="list-style-type: none"> <li>(1) R: Tape Reel</li> <li>(2) S08: SOP-8, CK08-2030: CDFN2030-8</li> <li>(3) G: Halogen Free and Lead Free, L: Lead Free</li> </ul>
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#### MARKING

SOP-8	CDFN2030-8
<p>UTC □□□□ → Date Code  L: Lead Free  G: Halogen Free  □□□□ → Lot Code</p>	<p>LVC 3G07 • □□□□ → Date Code</p>



■ PIN CONFIGURATION

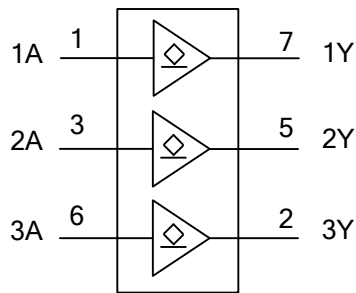


■ FUNCTION TABLE

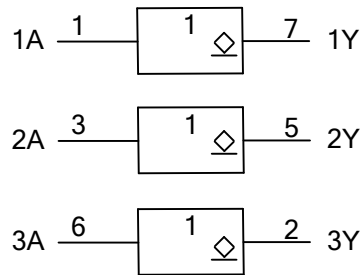
INPUT(A)	OUTPUT(Y)
L	L
H	Z

Note: H: High voltage level; L: Low voltage level.

■ LOGIC DIAGRAM (positive logic)



Logic symbol



IEC logic symbol

### ■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	$V_{CC}$		-0.5 ~ +6.5	V
Input Voltage	$V_{IN}$		-0.5 ~ +6.5	V
Output Voltage	$V_{OUT}$	Output in the high or low state	-0.5 ~ +6.5	V
		Output in the power-off state	-0.5 ~ +6.5	V
Continuous $V_{CC}$ or GND Current	$I_{CC}$		±100	mA
Continuous Output Current	$I_{OUT}$	$V_{OUT}=0V \sim V_{CC}$	±50	mA
Input Clamp Current	$I_{IK}$	$V_{IN}<0V$	-50	mA
Output Clamp Current	$I_{OK}$	$V_{OUT}>V_{CC}$ or $V_{OUT}<0V$	-50	mA
Storage Temperature Range	$T_{STG}$		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

### ■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	$V_{CC}$	Operating	1.65		5.5	V
		Data retention only	1.5			V
Input Voltage	$V_{IN}$		0		5.5	V
Output Voltage	$V_{OUT}$	High or low state	0		5.5	V
Operating Temperature (Note)	$T_A$		-40		+125	°C
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$	$V_{CC}=1.8V\pm 0.15V, 2.5V\pm 0.2V$			20	ns/V
		$V_{CC}=3.3V\pm 0.3V$			10	ns/V
		$V_{CC}=5V\pm 0.5V$			5	ns/V

Note: This condition is only determined from design. It can't be 100% tested in mass production.

### ■ ELECTRICAL CHARACTERISTICS ( $T_A=25^\circ C$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level Input Voltage	$V_{IH}$	$V_{CC}=1.8\pm 0.15V$	$0.65 \times V_{CC}$			V
		$V_{CC}=2.5\pm 0.2V$	1.7			V
		$V_{CC}=3.3\pm 0.3V$	2			V
		$V_{CC}=5\pm 0.5V$	$0.7 \times V_{CC}$			V
Low-level Input Voltage	$V_{IL}$	$V_{CC}=1.8\pm 0.15V$			$0.35 \times V_{CC}$	V
		$V_{CC}=2.5\pm 0.2V$			0.7	V
		$V_{CC}=3.3\pm 0.3V$			0.8	V
		$V_{CC}=5\pm 0.5V$			$0.3 \times V_{CC}$	V
Low-Level Output Voltage	$V_{OL}$	$V_{CC}=1.65 \sim 5.5V, I_{OL}=100\mu A$			0.1	V
		$V_{CC}=1.65V, I_{OL}=4mA$			0.45	V
		$V_{CC}=2.3V, I_{OL}=8mA$			0.3	V
		$V_{CC}=3.0V$ $I_{OL}=16mA$ $I_{OL}=24mA$			0.4	V
		$V_{CC}=4.5V, I_{OL}=32mA$			0.55	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=0 \sim 5.5V, V_{IN}=5.5V$ or GND			±5	μA
Power OFF Leakage Current	$I_{off}$	$V_{CC}=0V, V_{IN}$ or $V_{OUT}=5.5V$			±10	μA
3-state Output OFF-state Current	$I_{OZ}$	$V_{IN}=V_{IH}$ or $V_{IL}, V_{OUT}=V_{CC}$ or GND, $V_{CC}=5.5V$			±10	μA
Quiescent Supply Current	$I_{CC}$	$V_{CC}=1.65 \sim 5.5V,$ $V_{IN}=V_{CC}$ or GND, $I_{OUT}=0A$			10	μA
Additional Quiescent Supply Current Per Input Pin	$\Delta I_{CC}$	$V_{CC}=3 \sim 5.5V,$ One input at $V_{CC}-0.6V,$ Other inputs at $V_{CC}$ or GND			500	μA
Input Capacitance	$C_I$	$V_{CC}=3.3V, V_{IN}=V_{CC}$ or GND		3.5		pF

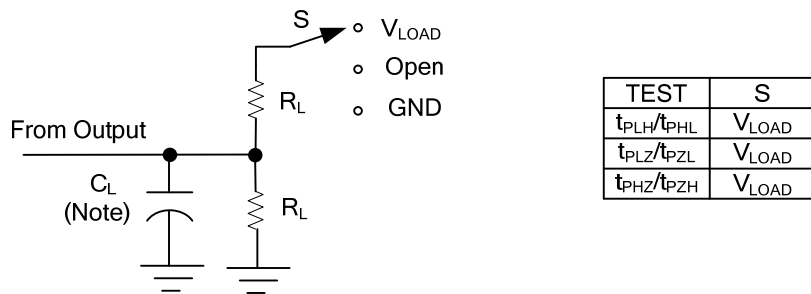
■ SWITCHING CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (A) to output(Y)	$t_{PZL} / t_{PLZ}$	$V_{CC}=1.8\pm 0.15\text{V}, C_L=30\text{pF}, R_L=1\text{k}\Omega$	1.5		7.8	ns
		$V_{CC}=2.5\pm 0.2\text{V}, C_L=30\text{pF}, R_L=500\Omega$	1.0		4.3	ns
		$V_{CC}=3.3\pm 0.3\text{V}, C_L=50\text{pF}, R_L=500\Omega$	1.1		3.7	ns
		$V_{CC}=5\pm 0.5\text{V}, C_L=50\text{pF}, R_L=500\Omega$	1.0		2.9	ns

■ OPERATING CHARACTERISTICS ( $f=10\text{MHz}, T_A = 25^\circ\text{C}$  , unless otherwise specified)

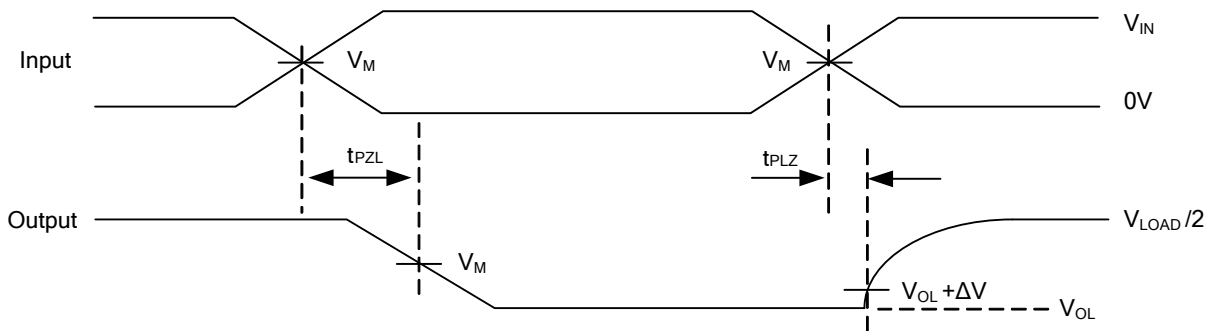
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	$C_{PD}$	$V_{CC}=1.8\text{V}$		3		pF
		$V_{CC}=2.5\text{V}$		3		pF
		$V_{CC}=3.3\text{V}$		4		pF
		$V_{CC}=5\text{V}$		5		pF

## ■ TEST CIRCUIT AND WAVEFORMS



Note:  $C_L$  includes probe and jig capacitance.

$V_{CC}$	Inputs		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_{IN}$	$t_R, t_F$					
$1.8V \pm 0.15V$	$V_{CC}$	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	30pF	1K $\Omega$	0.15V
$2.5V \pm 0.2V$	$V_{CC}$	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	30pF	500 $\Omega$	0.15V
$3.3V \pm 0.3V$	3V	$\leq 2.5ns$	1.5V	6V	50pF	500 $\Omega$	0.3V
$5V \pm 0.5V$	$V_{CC}$	$\leq 2.5ns$	$V_{CC}/2$	$2 \times V_{CC}$	50pF	500 $\Omega$	0.3V



- Notes: 1.  $C_L$  includes probe and jig capacitance.  
 2. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10MHz$ ,  $Z_o = 50\Omega$ .

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