

U74LVC2G241

CMOS IC

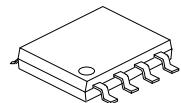
DUAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT

■ DESCRIPTION

The **U74LVC2G241** is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The **U74LVC2G241** is organized as two 1-bit line drivers with separate output-enable(\overline{OE} , $2OE$) inputs. When \overline{OE} is low and $2OE$ is high, the device passes data from the A inputs to the Y output. When \overline{OE} is high and $2OE$ is low, the output are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pull up resistor, and OE should be tied to GND through a pull down resistor, the minimum value of the resistor is determined by the current-sinking or the current-sourcing capability of the driver.



SOP-8

■ FEATURES

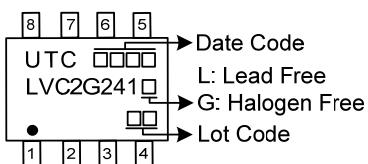
- * Wide supply voltage range from 1.65V to 5.5V
- * Inputs accept voltages up to 5.5V
- * I_{OFF} supports partial-power-down mode
- * Low static power consumption; $I_{CC}=10\mu A$ (Max.)

■ ORDERING INFORMATION

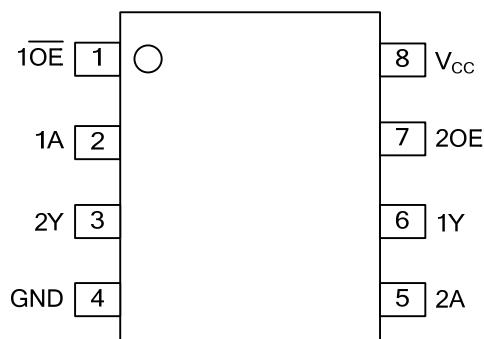
Ordering Number		Package	Packing
Free Plating	Halogen Free		
U74LVC2G241L-S08-R	U74LVC2G241G-S08-R	SOP-8	Tape Reel

U74LVC2G241G-S08-R 	(1)Packing Type (2)Package Type (3)Green Package (1) R: Tape Reel (2) S08: SOP-8 (3) G: Halogen Free and Lead Free
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■ MARKING



■ PIN CONFIGURATION



■ FUNCTION TABLE

INPUT(\overline{OE})	INPUT(1A)	OUTPUT(1Y)	INPUT(2OE)	INPUT(2A)	OUTPUT(2Y)
L	H	H	H	H	H
L	L	L	H	L	L
H	X	Z	L	X	Z

H = High voltage level ; L = Low voltage level ; X = Don't care ; Z = High-impedance OFF-state

■ LOGIC DIAGRAM (positive logic)



Logic symbol

■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V _{CC}		-0.5 ~ +6.5	V
Input Voltage	V _{IN}		-0.5 ~ +6.5	V
Output Voltage	V _{OUT}	Output in the high or low state	-0.5 ~ V _{CC} +0.5	V
		Output in the power-off state	-0.5 ~ +6.5	V
Continuous V _{CC} or GND Current	I _{CC}		±100	mA
Continuous Output Current	I _{OUT}	V _{OUT} =0V ~ V _{CC}	±50	mA
Input Clamp Current	I _{IK}	V _{IN} <0V	-50	mA
Output Clamp Current	I _{OK}	V _{OUT} >V _{CC} or V _{OUT} <0V	-50	mA
Storage Temperature Range	T _{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V _{CC}	Operating	1.65		5.5	V
		Data retention only	1.5			V
Input Voltage	V _{IN}		0		5.5	V
Output Voltage	V _{OUT}	High or low state	0		V _{CC}	V
Input Transition Rise or Fall Rate	Δt/Δv	V _{CC} =1.8V±0.15V, 2.5V±0.2V			20	ns/V
		V _{CC} =3.3V±0.3V			10	ns/V
		V _{CC} =5V±0.5V			5	ns/V
Operating Temperature	T _A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level Input Voltage	V _{IH}	V _{CC} =1.8±0.15V	0.65×V _{CC}			V
		V _{CC} =2.5±0.2V	1.7			V
		V _{CC} =3.3±0.3V	2			V
		V _{CC} =5±0.5V	0.7×V _{CC}			V
Low-level Input Voltage	V _{IL}	V _{CC} =1.8±0.15V			0.35×V _{CC}	V
		V _{CC} =2.5±0.2V			0.7	V
		V _{CC} =3.3±0.3V			0.8	V
		V _{CC} =5±0.5V			0.3×V _{CC}	V
High-Level Output Voltage	V _{OH}	V _{CC} =1.65 ~ 5.5V, I _{OH} =-100μA	V _{CC} -0.1			V
		V _{CC} =1.65V, I _{OH} =-4mA	1.2			V
		V _{CC} =2.3V, I _{OH} =-8mA	1.9			V
		V _{CC} =3.0V	I _{OH} =-16mA	2.4		V
			I _{OH} =-24mA	2.3		V
Low-Level Output Voltage	V _{OL}	V _{CC} =4.5V, I _{OL} =-32mA	3.8			V
		V _{CC} =1.65 ~ 5.5V, I _{OL} =100μA			0.1	V
		V _{CC} =1.65V, I _{OL} =4mA			0.45	V
		V _{CC} =2.3V, I _{OL} =8mA			0.3	V
		V _{CC} =3.0V	I _{OL} =16mA		0.4	V
			I _{OL} =24mA		0.55	V
		V _{CC} =4.5V, I _{OL} =32mA			0.55	V

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=0 \sim 5.5V, V_{IN}=5.5V \text{ or GND}$			± 5	μA
Power OFF Leakage Current	I_{off}	$V_{CC}=0V, V_{IN} \text{ or } V_{OUT}=5.5V$			± 10	μA
OFF-state output current	I_{OZ}	$V_{CC}=3.6V, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT}=5.5V \text{ or GND}$			10	μA
Quiescent Supply Current	I_{CC}	$V_{CC}=1.65 \sim 5.5V, V_{IN}=V_{CC} \text{ or GND}, I_{OUT}=0$			10	μA
Additional Quiescent Supply Current Per Input Pin	ΔI_{CC}	$V_{CC}=3 \sim 5.5V, \text{ One input at } V_{CC}-0.6V, \text{ Other inputs at } V_{CC} \text{ or GND}$			500	μA
Input Capacitance	C_I	$V_{CC}=3.3V, V_{IN}=V_{CC} \text{ or GND}$		3.5		pF
Output Capacitance	C_O	$V_{CC}=3.3V, V_{OUT}=V_{CC} \text{ or GND}$		6.5		pF

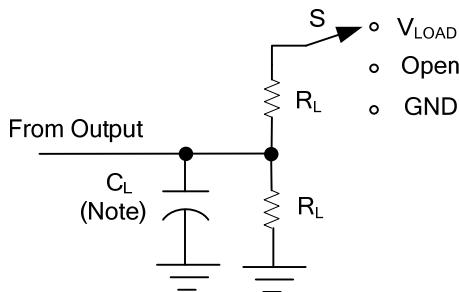
■ SWITCHING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from inputs (A) to output(Y)	t_{PD}	$V_{CC}=1.8 \pm 0.15V, C_L=30pF, R_L=1k\Omega$	3.3		8.8	ns
		$V_{CC}=2.5 \pm 0.2V, C_L=30pF, R_L=500\Omega$	1.5		4.8	ns
		$V_{CC}=3.3 \pm 0.3V, C_L=50pF, R_L=500\Omega$	1.4		4.3	ns
		$V_{CC}=5 \pm 0.5V, C_L=50pF, R_L=500\Omega$	1		3.7	ns
Propagation delay from input (\overline{OE}) to output(Y)	t_{en}	$V_{CC}=1.8 \pm 0.15V, C_L=30pF, R_L=1k\Omega$	4		9.9	ns
		$V_{CC}=2.5 \pm 0.2V, C_L=30pF, R_L=500\Omega$	1.9		5.6	ns
		$V_{CC}=3.3 \pm 0.3V, C_L=50pF, R_L=500\Omega$	1.2		4.7	ns
		$V_{CC}=5 \pm 0.5V, C_L=50pF, R_L=500\Omega$	1.2		3.8	ns
Propagation delay from input (\overline{OE}) to output(Y)	t_{dis}	$V_{CC}=1.8 \pm 0.15V, C_L=30pF, R_L=1k\Omega$	1.5		11.6	ns
		$V_{CC}=2.5 \pm 0.2V, C_L=30pF, R_L=500\Omega$	1		5.8	ns
		$V_{CC}=3.3 \pm 0.3V, C_L=50pF, R_L=500\Omega$	1.4		4.4	ns
		$V_{CC}=5 \pm 0.5V, C_L=50pF, R_L=500\Omega$	1		3.4	ns
Propagation delay from input (\overline{OE}) to output(Y)	t_{en}	$V_{CC}=1.8 \pm 0.15V, C_L=30pF, R_L=1k\Omega$	3.2		8.8	ns
		$V_{CC}=2.5 \pm 0.2V, C_L=30pF, R_L=500\Omega$	1.5		4.7	ns
		$V_{CC}=3.3 \pm 0.3V, C_L=50pF, R_L=500\Omega$	1.6		4.1	ns
		$V_{CC}=5 \pm 0.5V, C_L=50pF, R_L=500\Omega$	1.1		3.3	ns
Propagation delay from input (\overline{OE}) to output(Y)	t_{dis}	$V_{CC}=1.8 \pm 0.15V, C_L=30pF, R_L=1k\Omega$	1.7		12.5	ns
		$V_{CC}=2.5 \pm 0.2V, C_L=30pF, R_L=500\Omega$	1		5.2	ns
		$V_{CC}=3.3 \pm 0.3V, C_L=50pF, R_L=500\Omega$	1		4.2	ns
		$V_{CC}=5 \pm 0.5V, C_L=50pF, R_L=500\Omega$	1		3.3	ns

■ OPERATING CHARACTERISTICS (f=10MHz, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	Output enabled	$V_{CC}=1.8V$		19		pF
		$V_{CC}=2.5V$		19		pF
		$V_{CC}=3.3V$		20		pF
		$V_{CC}=5V$		22		pF
	Output disabled	$V_{CC}=1.8V$		2		pF
		$V_{CC}=2.5V$		2		pF
		$V_{CC}=3.3V$		2		pF
		$V_{CC}=5V$		3		pF

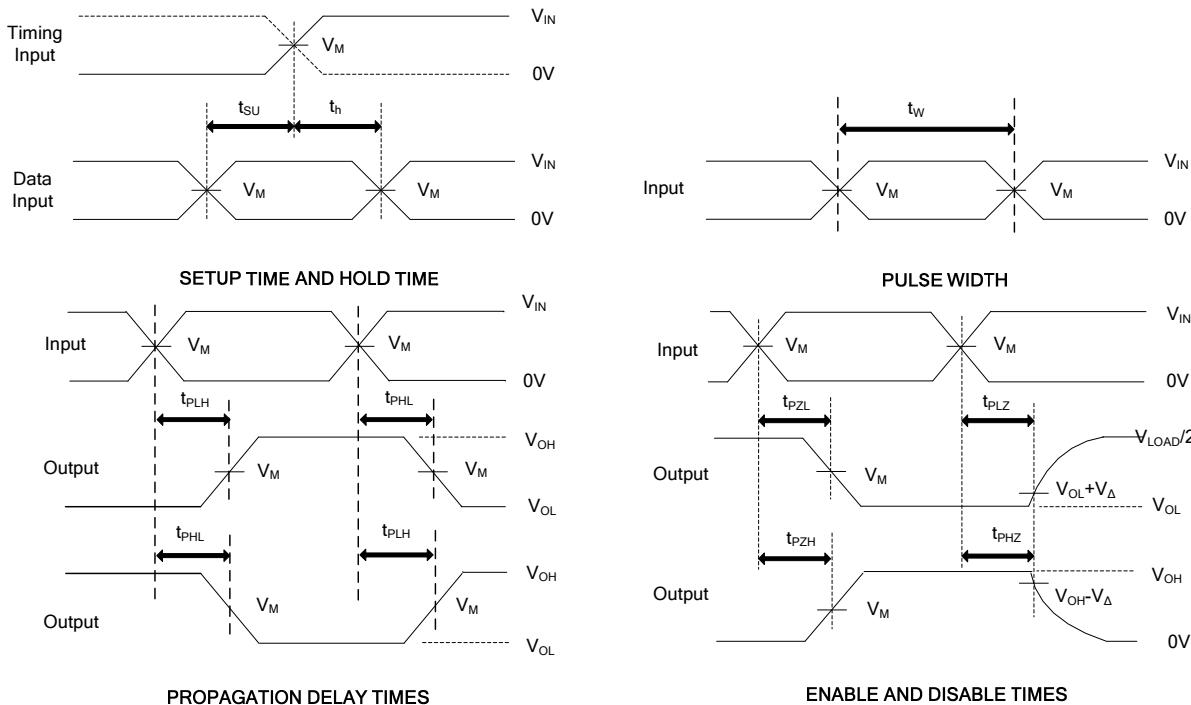
■ TEST CIRCUIT AND WAVEFORMS



TEST	S
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

Note: C_L includes probe and jig capacitance.

V_{CC}	V_{IN}	t_R / t_F	V_M	V_{LOAD}	C_L	R_L	V_Δ
$1.8V \pm 0.15V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	$30pF$	$1K\Omega$	$0.15V$
$2.5V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	$30pF$	500Ω	$0.15V$
$3.3V \pm 0.3V$	$3V$	$\leq 2.5ns$	$1.5V$	$6V$	$50pF$	500Ω	$0.3V$
$5V \pm 0.5V$	V_{CC}	$\leq 2.5ns$	$V_{CC}/2$	$2 \times V_{CC}$	$50pF$	500Ω	$0.3V$



Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10MHz$, $Z_O = 50\Omega$.

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