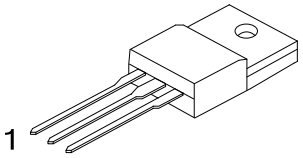
UF730K-MT

Preliminary | ***Power MOSFET***

5.5A, 400V N-CHANNEL POWER MOSFET



TO-220F1

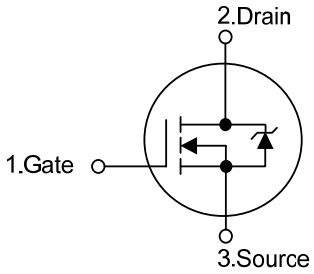
■ DESCRIPTION

The N-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications such as switching regulators, switching converters, solenoid, motor drivers, relay drivers.

■ FEATURES

* $R_{DS(ON)}$ < 0.95Ω @ V_{GS}=10V, I_D=3.0A
* Avalanche Energy Specified
* Rugged - SOA is Power Dissipation Limited
* Fast Switching Capability
* Linear Transfer Characteristics
* High Input Impedance

■ SYMBOL



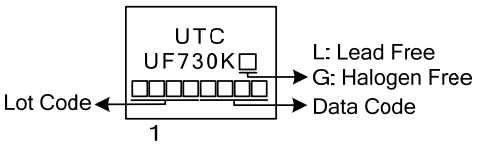
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UF730KL-TF1-T	UF730KG-TF1-T	TO-220F1	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

UF730KL-TF1-T (1)Packing Type (2)Package Type (3)Green Package	(1) T: Tube (2) TF1: TO220F1 (3) L: Lead Free, G: Halogen Free and Lead Free

■ MARKING



■ ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	400	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (T_J =25°C ~125°C)		V_{DGR}	400	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current		I_D	5.5	A
Pulsed Drain Current (Note 2)		I_{DM}	22	A
Single Pulse Avalanche Energy (Note 3)		E_{AS}	300	mJ
Power Dissipation	T_C = 25°C	P_D	35	W
	Derate above 25°C		0.28	W
Junction Temperature		T_J	+150	°C
Storage Temperature		T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating : Pulse width limited by maximum junction temperature.
3. L = 20mH, I_{AS} = 5.5A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
4. I_{SD}≤5.5A, di/dt≤100A/μs, V_{DD}≤BV_{DSS}, T_J≤T_{JMAX}

■ THERMAL DATA

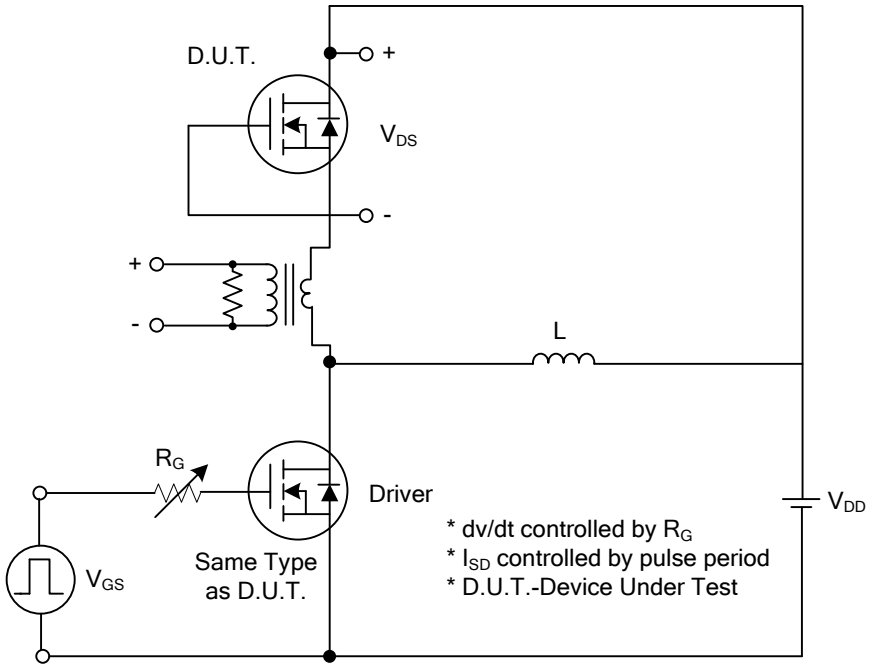
PARAMETER	SYMBOL	RATINGS	UNIT
Junction-to-Ambient	θ_{JA}	62.5	°C/W
Junction-to-Case	θ_{JC}	3.6	°C/W

■ ELECTRICAL CHARACTERISTICS (T_C =25°C, unless otherwise specified.)

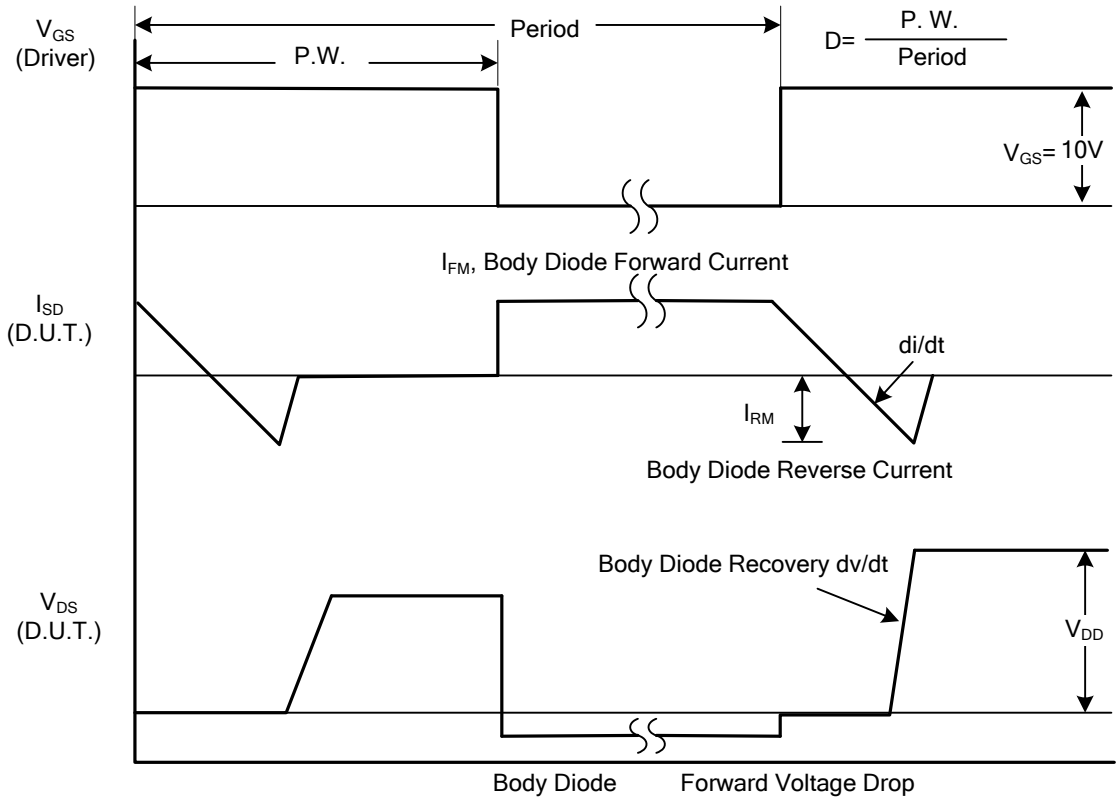
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	400			V
On-State Drain Current (Note 1)	$I_{D(ON)}$	V_{DS}>$I_{D(ON)}$×$R_{DS(ON)MAX}$, V_{GS}=10V	5.5			A
Drain-Source Leakage Current	I_{DSS}	V_{DS}=Rated BV_{DSS}, V_{GS}=0V			25	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=3.0A			0.95	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	V_{DS}=25V, V_{GS}=0V, f=1MHz		810		pF
Output Capacitance	C_{OSS}			1200		pF
Reverse Transfer Capacitance	C_{RSS}			300		pF
SWITCHING CHARACTERISTICS						
Total Gate Charge	Q_G	V_{GS}=50V, I_D=1.3A, V_{DS}=10V, I_G=100μA		18		nC
Gate-Source Charge	Q_{GS}			6		nC
Gate-Drain Charge	Q_{GD}			4		nC
Turn-On Delay Time	$t_{D(ON)}$	V_{DD}=30V, I_D≈0.5A, V_{GS}=0~10V, R_G=25Ω (Note 1, 2)		50		ns
Turn-On Rise Time	t_R			51		ns
Turn-Off Delay Time	$t_{D(OFF)}$			100		ns
Turn-Off Fall Time	t_F			45		ns
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_{SD}=5.5A			1.6	V
Maximum Continuous Drain-Source Diode Forward Current	I_S				5.5	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				22	A
Reverse Recovery Time	t_{RR}	I_{SD} = 5.5A, dI_{SD}/dt = 100A/μs (Note 1)		300		ns
Reverse Recovery Charge	Q_{RR}			2.1		μC

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



Peak Diode Recovery dv/dt Test Circuit



Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

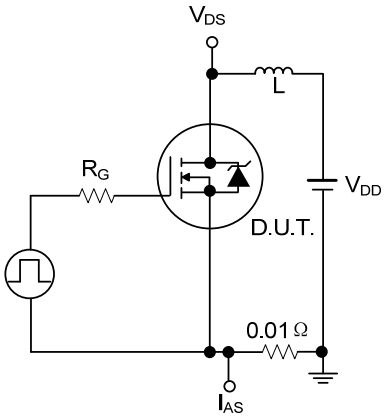


Figure 1A. Unclamped Energy Test Circuit

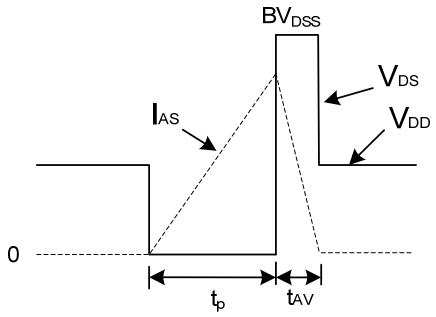


Figure 1B. Unclamped Energy Waveforms

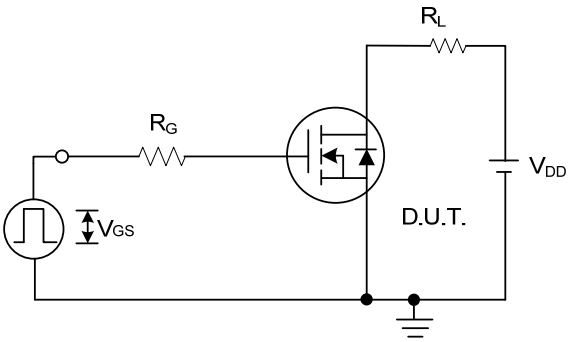


Figure 2A. Switching Time Test Circuit

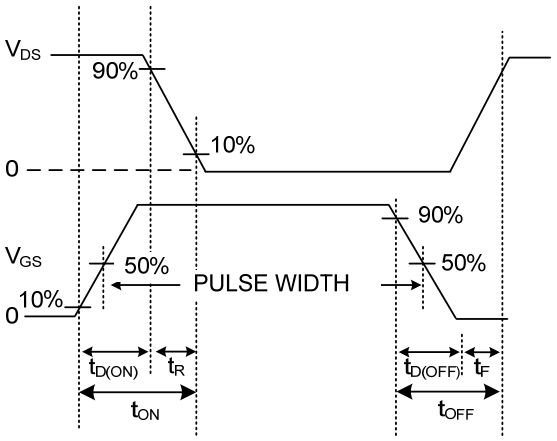


Figure 2B. Resistive Switching Waveforms

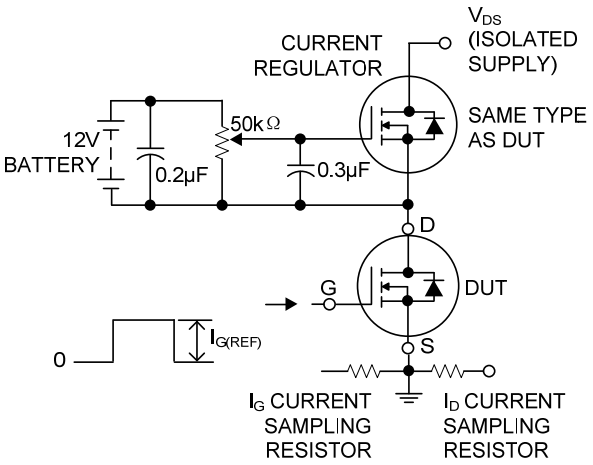


Figure 3A. Gate Charge Test Circuit

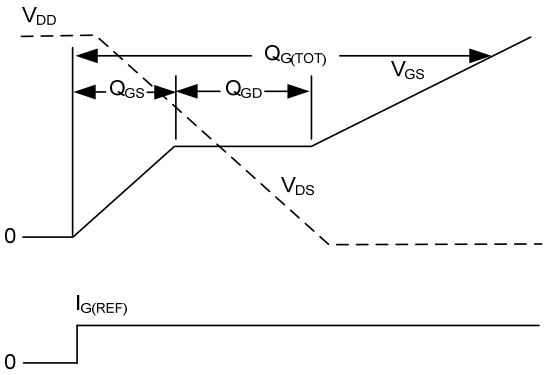


Figure 3B. Gate Charge Waveforms