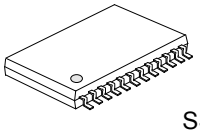
16-BIT CONSTANT CURRENT LED SINK DRIVER



SSOP-24
(150mil)

■ DESCRIPTION

The UTC **L16B45A** is designed for LED displays. UTC **L16B45A** contains a serial buffer and data latches which convert serial input data into parallel output format. At UTC **L16B45A** output stage, sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LEDs within a large range of V_f variations.

UTC **L16B45A** provides users with great flexibility and device performance while using UTC **L16B45A** in their system design for LED display applications, e.g. LED panels. Users may adjust the output current from 3mA to 45mA through an external resistor, R_{ext}, which gives users flexibility in controlling the light intensity of LEDs. UTC **L16B45A** guarantees to endure maximum 17V at the output port. The high clock frequency, 25MHz, also satisfies the system requirements of high volume data transmission.

■ FEATURES

* 16 constant-current output channels
* Constant output current invariant to load voltage change
  Constant output current range:
  3~45mA @ V_{DD}=5V
  3~30mA @ V_{DD}=3.3V
* Excellent output current accuracy:
  between channels: ±2.5% (max.),
  between ICs: ±3.0% (max.)
* Output current adjusted through an external resistor
* Fast response of output current, $\overline{OE}$ (min.): 70ns @ V_{DD}=3.3V
* 25MHz clock frequency
* Schmitt trigger input
* 3.3V/5V supply voltage
* Halogen Free

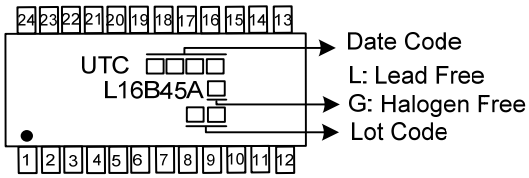
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
L16B45AL-R24-R	L16B45AG-R24-R	SSOP-24	Tape Reel

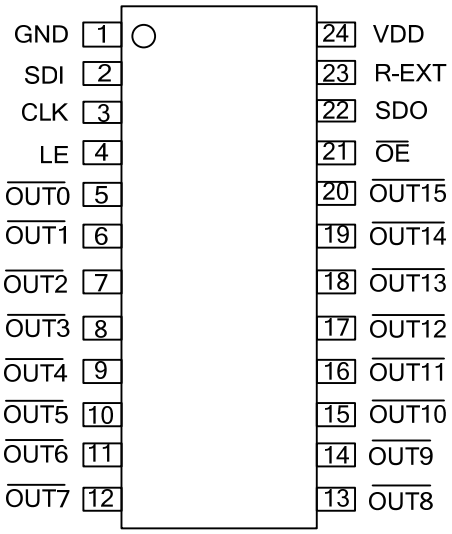
L16B45AG-R24-R

(1) Packing Type	(1) R: Tape Reel
(2) Package Type	(2) R24: SSOP-24
(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



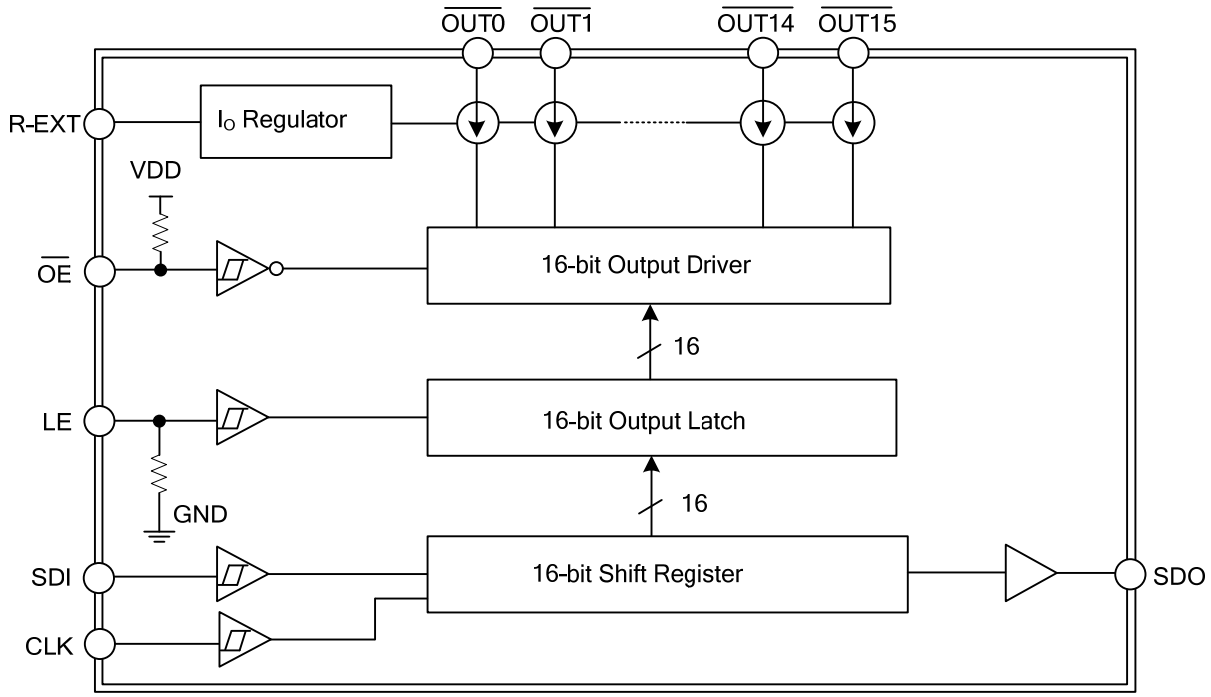
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	GND	Ground terminal for control logic and current sink
2	SDI	Serial-data input to the shift register
3	CLK	Clock input terminal for data shift on rising edge
4	LE	Data strobe input terminal Serial data is transferred to the output latch when LE is high. The data is latched when LE goes low.
5~20	$\overline{OUT0}$ ~ $\overline{OUT15}$	Constant current output terminals
21	$\overline{OE}$	Output enable terminal When (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked).
22	SDO	Serial-data output to the following SDI of next driver IC
23	R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
24	V_{DD}	3.5V/5V supply voltage terminal

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	0 ~ 7.0	V
Input Voltage	V_{IN}	-0.4 ~ V_{DD}+0.4	V
Output Current	I_{OUT}	+45	mA
Output Voltage	V_{DS}	-0.5 ~ +17.0	V
GND Terminal Current	I_{GND}	720	mA
Power Dissipation (On PCB, T_A=25°C)	P_D	1.37	W
Thermal Resistance (On PCB, T_A=25°C)	θ_{JA}	91	°C/W
Junction Temperature	T_J	+150	°C
Operating Temperature	T_{OPR}	-40 ~ +85	°C
Storage Temperature	T_{STG}	-55 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ DC ELECTRICAL CHARACTERISTICS (V_{DD}=5.0V)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage		V_{DD}		4.5	5.0	5.5	V
Output Voltage		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$			17.0	V
Output Current		I_{OUT}	DC Test Circuit	3		45	mA
		I_{OH}	SDO			-1.0	mA
		I_{OL}	SDO			1.0	mA
Input Voltage	"H" Level	V_{IH}	T_A=-40~85°C	0.7×V_{DD}		V_{DD}	V
	"L" Level	V_{IL}	T_A=-40~85°C	GND		0.3×V_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V		0.5		μA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		0.4		V
		V_{OH}	I_{OH}=-1.0mA		4.6		V
Output Current 1		I_{OUT1}	V_{DS}=1.0V, R_{EXT}=6000Ω		3.1		mA
Current Skew		dI_{OUT1}	I_{OL}=3.1mA, V_{DS}=1.0V, R_{EXT}=6000Ω		±2.5		%
Output Current 2		I_{OUT2}	V_{DS}=1.0V, R_{EXT}=720Ω		25.8		mA
Current Skew		dI_{OUT2}	I_{OL}=25.8mA, V_{DS}=1.0V, R_{EXT}=720Ω		±2		%
Output Current vs. Output Voltage Regulation		%/dV_{DS}	V_{DS}=1.0~3.0V		±0.1		%/V
Output Current vs. Supply Voltage Regulation		%/dV_{DD}	V_{DD}=4.5~5.5V		±1.0		%/V
Pull-Up Resistor		R_{IN}(up)	$\overline{OE}$	250	500	800	KΩ
Pull-Down Resistor		R_{IN}(down)	LE	250	500	800	KΩ
Supply Current	"OFF"	I_{DD}(off) 1	R_{EXT}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		2	2.8	mA
		I_{DD}(off) 2	R_{EXT}=1240Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		4	4.8	mA
		I_{DD}(off) 3	R_{EXT}=620Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		6	6.8	mA
	"ON"	I_{DD}(on) 1	R_{EXT}=1240Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		5.2	8.2	mA
		I_{DD}(on) 2	R_{EXT}=620Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		6.5	9.5	mA

■ DC ELECTRICAL CHARACTERISTICS (V_{DD}=3.3V)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage		V_{DD}		3.0	3.3	4.5	V
Output Voltage		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$			17.0	V
Output Current		I_{OUT}	DC Test Circuit	3		30	mA
		I_{OH}	SDO			-1.0	mA
		I_{OL}	SDO			1.0	mA
Input Voltage	"H" Level	V_{IH}	T_A=-40~85°C	0.7×V_{DD}		V_{DD}	V
	"L" Level	V_{IL}	T_A=-40~85°C	GND		0.3×V_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V		0.5		μA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		0.4		V
		V_{OH}	I_{OH}=-1.0mA		2.9		V
Output Current 1		I_{OUT1}	V_{DS}=1.0V, R_{EXT}=6000Ω		3.1		mA
Current Skew		dI_{OUT1}	I_{OL}=3.1mA, V_{DS}=1.0V, R_{EXT}=6000Ω		±2.5		%
Output Current 2		I_{OUT2}	V_{DS}=1.0V, R_{EXT}=720Ω		25.8		mA
Current Skew		dI_{OUT2}	I_{OL}=25.8mA, V_{DS}=1.0V, R_{EXT}=720Ω		±2		%
Output Current vs. Output Voltage Regulation		%/dV_{DS}	V_{DS}=1.0~3.0V		±0.1		%/V
Output Current vs. Supply Voltage Regulation		%/dV_{DD}	V_{DD}=3.0~3.6V		±1.0		%/V
Pull-Up Resistor		R_{IN}(up)	$\overline{OE}$	250	500	800	KΩ
Pull-Down Resistor		R_{IN}(down)	LE	250	500	800	KΩ
Supply Current	"OFF"	I_{DD}(off) 1	R_{EXT}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		1.7	2.3	mA
		I_{DD}(off) 2	R_{EXT}=1851Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		3.9	4.5	mA
		I_{DD}(off) 3	R_{EXT}=748Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		5.2	5.8	mA
	"ON"	I_{DD}(on) 1	R_{EXT}=1851Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		3.9	5.0	mA
		I_{DD}(on) 2	R_{EXT}=748Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		5.2	5.8	mA

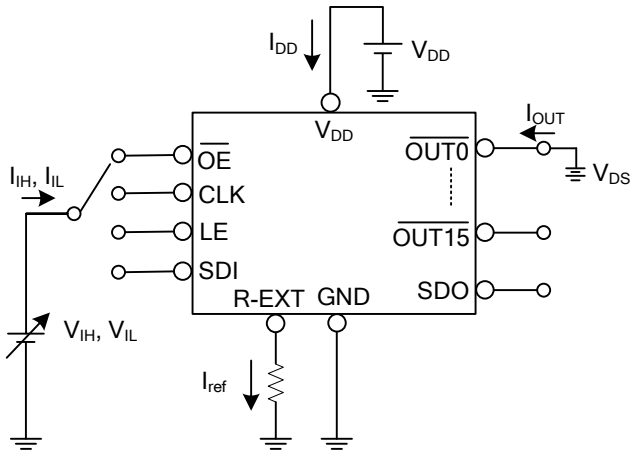
■ SWITCHING ELECTRICAL CHARACTERISTICS (V_{DD}=5.0V)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time (“L” to “H”)	CLK- $\overline{OUT2n}$	t_{pLH1}	V_{DD}=5.0V, V_{DS}=1.0V, V_{IH}=V_{DD}, V_{IL}=GND R_{ext}=930Ω, V_L=4.5V, R_L=162Ω, C_L=10pF		50	70	ns
	CLK- $\overline{OUT2n+1}$				35	55	ns
	LE- $\overline{OUT2n}$	t_{pLH2}			50	70	ns
	LE- $\overline{OUT2n+1}$				35	55	ns
	$\overline{OE}$ - $\overline{OUT2n}$	t_{PLH3}			50	70	ns
	$\overline{OE}$ - $\overline{OUT2n+1}$				35	55	ns
	CLK-SDO	t_{PLH}			20	40	ns
Propagation Delay Time (“H” to “L”)	CLK- $\overline{OUT2n}$	t_{pHL1}			90	110	ns
	CLK- $\overline{OUT2n+1}$				75	95	ns
	LE- $\overline{OUT2n}$	t_{pHL2}			90	110	ns
	LE- $\overline{OUT2n+1}$				75	95	ns
	$\overline{OE}$ - $\overline{OUT2n}$	t_{pHL3}			90	110	ns
	$\overline{OE}$ - $\overline{OUT2n+1}$				75	95	ns
	CLK-SDO	t_{pHL}			20	40	ns
Pulse Width	CLK	$t_{w(CLK)}$		20			ns
	LE	$t_{w(L)}$		20			ns
	$\overline{OE}$	$t_{w(OE)}$		70	100		ns
Hold Time for LE		$t_{h(L)}$		30			ns
Setup Time for LE		$t_{su(L)}$		5			ns
Hold Time for SDI		$t_{h(D)}$		5			ns
Setup Time for SDI		$t_{su(D)}$		3			ns
Maximum CLK Rise Time		t_r				500	ns
Maximum CLK Fall Time		t_f				500	ns
SDO Rise Time		$t_{r, SDO}$			10		ns
SDI Fall Time		$t_{f, SDO}$			10		ns
Output Rise Time of I_{OUT}		t_{or}			40		ns
Output Fall Time of I_{OUT}		t_{of}			55		ns

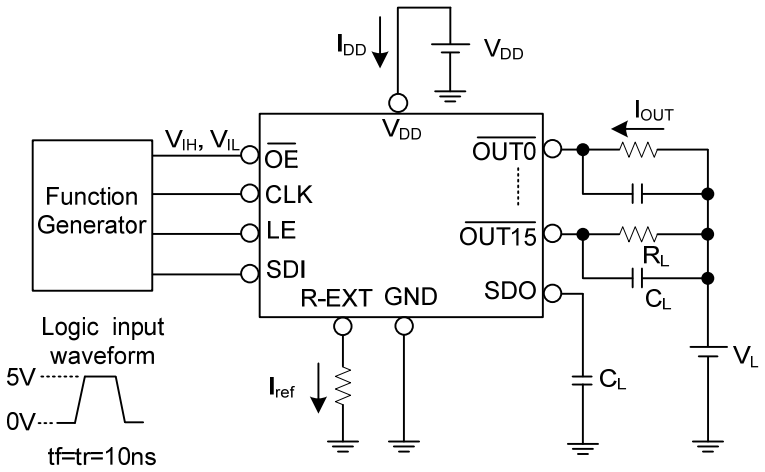
■ SWITCHING ELECTRICAL CHARACTERISTICS (V_{DD}=3.3V)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time (“L” to “H”)	CLK- $\overline{OUT2n}$	t_{pLH1}	V_{DD}=3.3V, V_{DS}=1.0V, V_{IH}=V_{DD}, V_{IL}=GND R_{ext}=930Ω, V_L=3.0V, R_L=100Ω, C_L=10pF		50	70	ns
	CLK- $\overline{OUT2n+1}$				35	55	ns
	LE- $\overline{OUT2n}$	t_{pLH2}			50	70	ns
	LE- $\overline{OUT2n+1}$				35	55	ns
	$\overline{OE}$ - $\overline{OUT2n}$	t_{PLH3}			50	70	ns
	$\overline{OE}$ - $\overline{OUT2n+1}$				35	55	ns
	CLK-SDO	t_{PLH}			20	40	ns
Propagation Delay Time (“H” to “L”)	CLK- $\overline{OUT2n}$	t_{pHL1}			115	135	ns
	CLK- $\overline{OUT2n+1}$				100	120	ns
	LE- $\overline{OUT2n}$	t_{pHL2}			115	135	ns
	LE- $\overline{OUT2n+1}$				100	120	ns
	$\overline{OE}$ - $\overline{OUT2n}$	t_{pHL3}			105	125	ns
	$\overline{OE}$ - $\overline{OUT2n+1}$				90	110	ns
	CLK-SDO	t_{pHL}			20	40	ns
Pulse Width	CLK	$t_{w(CLK)}$		20			ns
	LE	$t_{w(L)}$		20			ns
	$\overline{OE}$	$t_{w(OE)}$		100	130		ns
Hold Time for LE		$t_{h(L)}$		30			ns
Setup Time for LE		$t_{su(L)}$		5			ns
Hold Time for SDI		$t_{h(D)}$		5			ns
Setup Time for SDI		$t_{su(D)}$		3			ns
Maximum CLK Rise Time		t_r				500	ns
Maximum CLK Fall Time		t_f				500	ns
SDO Rise Time		$t_{r, SDO}$			10		ns
SDI Fall Time		$t_{f, SDO}$			10		ns
Output Rise Time of I_{OUT}		t_{or}			40		ns
Output Fall Time of I_{OUT}		t_{of}			65		ns

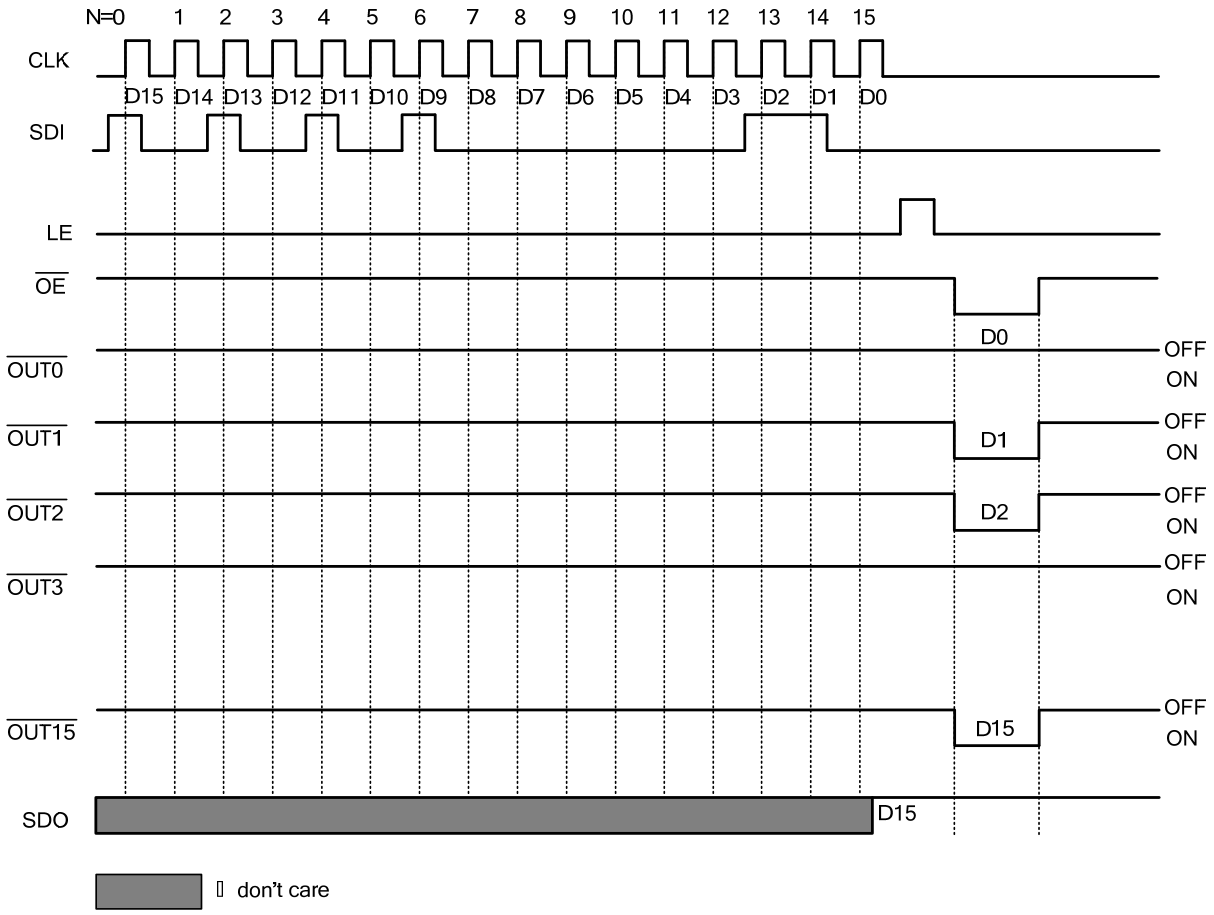
■ TEST CIRCUIT FOR DC ELECTRICAL CHARACTERISTICS



■ TEST CIRCUIT FOR SWITCHING ELECTRICAL CHARACTERISTICS



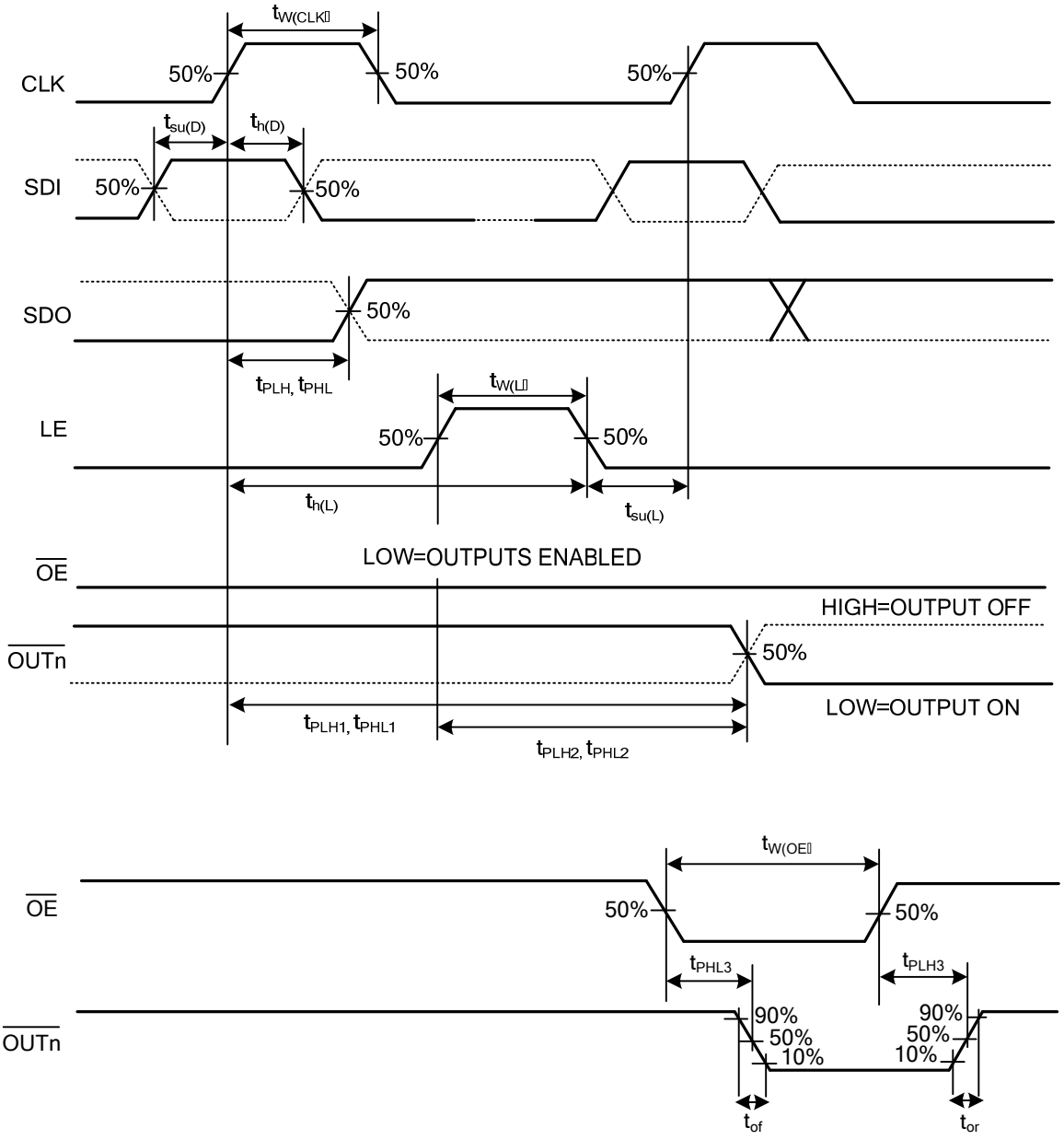
■ TIMING DIAGRAM



■ TRUTH TABLE

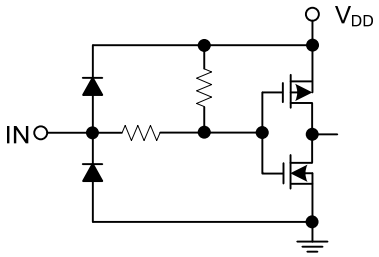
CLK	LE	$\overline{OE}$	SDI	$\overline{OUT0}$ … $\overline{OUT7}$ … $\overline{OUT15}$	SDO
↑	H	L	D_n	$\overline{Dn}$ …… $\overline{Dn-7}$ …. $\overline{Dn-15}$	D_{n-15}
↑	L	L	D_{n+1}	No Change	D_{n-14}
↑	H	L	D_{n+2}	$\overline{Dn+2}$ …… $\overline{Dn-5}$ …. $\overline{Dn-13}$	D_{n-13}
↓	X	L	D_{n+3}	$\overline{Dn+2}$ …… $\overline{Dn-5}$ …. $\overline{Dn-13}$	D_{n-13}
↓	X	H	D_{n+3}	Off	D_{n-13}

■ TIMING WAVEFORM

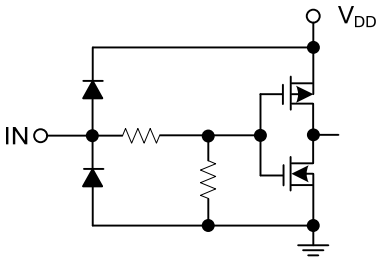


■ EQUIVALENT CIRCUITS OF INPUTS AND OUTPUTS

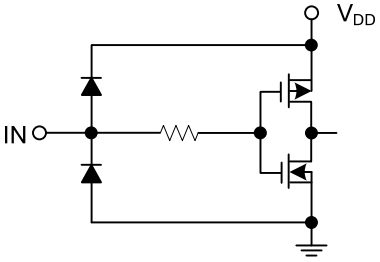
$\overline{OE}$ terminal



LE terminal



CLK, SDI terminal



SDO terminal