



LC1111

Advance

LINEAR INTEGRATED CIRCUIT

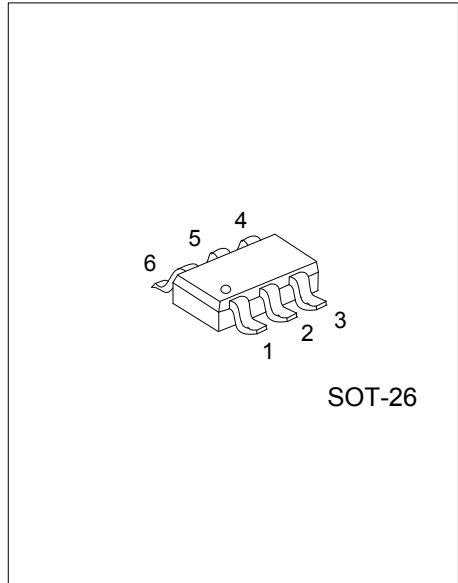
LOW DROPOUT LINEAR REGULATOR CONTROLLER

DESCRIPTION

The UTC **LC1111** is a low dropout linear regulator controller for applications requiring high-current and ultra low dropout voltages. The use of an external N-Channel MOSFET and provide an adjustable output by using an external resistive divider.

An extremely accurate 0.8V ($\pm 2\%$) reference allows the implementation of sub 1 V voltage supplies. The reference is guaranteed over the complete supply and temperature ranges.

The UTC **LC1111** integrates various functions. For example, a Power-On-Reset (POR) circuit monitors V_{CC} supply voltage to prevent wrong operations; the function of Under-Voltage Protection (UVP) protects the device from short circuit condition. The soft-start of output voltage is adjustable by the external capacitor on SS pin. Moreover, the UTC **LC1111** can be enabled by other power system; namely, holding the EN above 1.6V enables output and pulling the EN under 0.4 disables output.



SOT-26

FEATURES

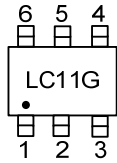
- * 4.5V~13.5V supply voltage range
- * 0.8V ($\pm 2\%$) voltage reference (temperature and process)
- * Power-On-Reset monitoring on V_{CC}
- * Fast transient response
- * Programmable soft-start
- * Enable control function
- * Low shutdown current
- * Under-Voltage protection
- * Two versions of IC available: UVP activated after V_{OUT} is ready

ORDERING INFORMATION

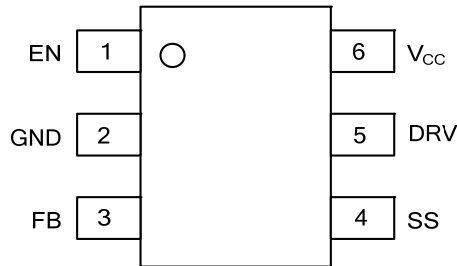
Ordering Number	Package	Packing
LC1111G-AG6-R	SOT-26	Tape Reel

<p>LC1111G-AG6-R</p> <pre> graph TD A[LC1111G-AG6-R] --- B["(1)Packing Type"] A --- C["(2)Package Type"] A --- D["(3)Green Package"] </pre>	<p>(1) R: Tape Reel</p> <p>(2) AG6: SOT-26</p> <p>(3) G: Halogen Free and Lead Free</p>
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■ MARKING



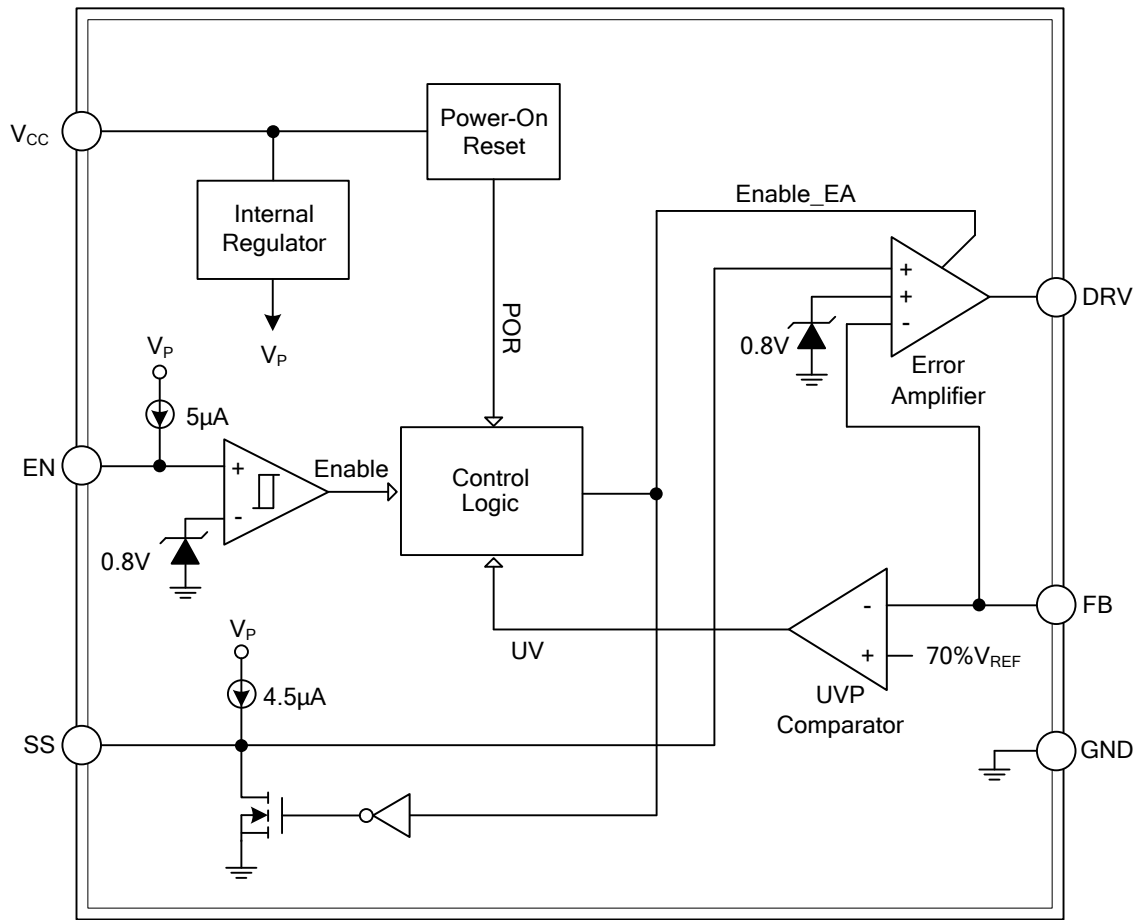
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	EN	Enable control pin. Pulling the EN high ($V_{EN} > 1.6$) enables the V_{OUT} ; forcing the EN low ($V_{EN} < 0.4V$) disables the V_{OUT} . When re-enabled, the IC undergoes a new soft-start process. The EN pin is pulled high internally, hence it can be left open if the EN control is not used.
2	GND	Ground pin of the circuitry. All voltage levels are measured with respect to this pin.
3	FB	Voltage Feedback Pin. Connecting this pin to an external resistor divider receives the feedback voltage of the regulator.
4	SS	Connect this pin to a capacitor for soft-start.
5	DRV	This pin drives the gate of an external N-channel MOSFET for linear regulator.
6	V_{CC}	Power input pin of the device. The voltage at this pin is monitored for Power-On-Reset purpose.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
V _{CC} Input Voltage (V _{CC} to GND)	V _{CC}	-0.3~16	V
EN, SS, to GND Voltage		-0.3~7	V
FB to GND Voltage	V _{FB}	-0.3~7	V
DRV to GND Voltage	V _{DRV}	-0.3~V _{CC} +0.3	V
Junction Temperature	T _J	150	°C
Storage Temperature	T _{STG}	-65~150	°C
Maximum Lead Soldering Temperature, 10 Seconds	T _{SDR}	260	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL CHARACTERISTIC

PARAMETER	SYMBOL	TYPICAL VALUE	UNIT
Junction-to-Ambient Resistance in Free Air (Note 1)	θ_{JA}	250	°C/W

■ RECOMMENDED OPERATING CONDITIONS (Note 2)

PARAMETER	SYMBOL	RATINGS	UNIT
V _{CC} Input Voltage (V _{CC} to GND)	V _{CC}	4.5~13.5	V
EN to GND Voltage	V _{EN}	0~5.5	V
V _{OUT} Output Voltage (Note 3)	V _{OUT}	0.8~V _{IN} -V _{DROP}	V
Ambient Temperature	T _A	-40~85	°C
Junction Temperature	T _J	-40~125	°C

Notes: 1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.
 2. Refer to the typical application circuit.
 3. V_{DROP} defined as the V_{IN} - V_{OUT} voltage at V_{OUT}=98% normal V_{OUT}. The linear regulator must provide the output MOSFET with sufficient Gate-to-Source voltage (V_{GS}=V_{CC}-V_{OUT}) to regulate the output voltage.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, these specifications apply over $V_{CC}=5/12V$, $T_A=-40\sim 85^{\circ}C$. Typical values are at $T_A=25^{\circ}C$.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{CC} Supply Current	I_{CC}	$V_{CC}=12V$		0.8	1.0	mA
		$V_{CC}=5V$		0.8	1.0	mA
V_{CC} Shutdown Current	I_{SD}	$V_{CC}=12V, EN=GND$			5	μA
		$V_{CC}=5V, EN=GND$			5	μA
POWER-ON-RESET (POR)						
V_{CC} POR Threshold		V_{CC} Risig	3.8	4.0	4.2	V
V_{CC} POR Hysteresis				0.4		V
REFERENCE VOLTAGE						
Reference Voltage	V_{REF}	$V_{CC}=12V, T_A=25^{\circ}C$		0.8		V
Reference Voltage Accuracy		$V_{CC}=12V$	-1		1	%
Line Regulation		$V_{CC}=4.5V\sim 13.2V$	-1.5		1.5	%
FB Input Current			-100		100	nA
ERROR AMPLIFIER						
Unity Gain Bandwidth		$V_{CC}=5/12V$		2		MHz
Open Loop DC Gain		$V_{CC}=12V, No\ Load$	60	80		dB
Power Supply Rejection Ratio	PSRR	$V_{CC}=12V, 100Hz, No\ Load$	50			dB
DRV High Voltage	$V_{DRV (high)}$	$V_{CC}=12V, I_{DRV (SOURCE)}=5mA, V_{FB}=0.6V$	11.2	11.5		V
		$V_{CC}=5V, I_{DRV (SOURCE)}=5mA, V_{FB}=0.6V$		4.7		V
DRV Low Voltage	$V_{DRV (low)}$	$V_{CC}=12V, I_{DRV (SINK)}=5mA, V_{FB}=1V$		0.5	1	V
		$V_{CC}=5V, I_{DRV (SINK)}=5mA, V_{FB}=1V$		0.8		V
DRV Source Current	$I_{DRV (source)}$	$V_{CC}=12V, V_{DRV}=6V, V_{FB}=0.6V$		50		mA
		$V_{CC}=5V, V_{DRV}=2.5V, V_{FB}=0.6V$		10		mA
DRV Sink Current	$I_{DRV (sink)}$	$V_{CC}=12V, V_{DRV}=6V, V_{FB}=1V$		40		mA
		$V_{CC}=5V, V_{DRV}=2.5V, V_{FB}=1V$		10		mA
ENABLE						
EN Logic High Threshold Voltage	$V_{EN (TH)}$	V_{EN} Rising	0.55	0.8	1.05	V
EN Hysteresis				50		mV
EN Shutdown Debounce		V_{EN} Falling		2		μs
EN Internal Pull High Current				5		μA
SOFT-START						
SS Current	I_{SS}			4.5		μA
UNDER-VOLTAGE PROTECTION (UVP)						
Under-Voltage Threshold	$V_{UV (TH)}$	$V_{EN}=5V, V_{FB}$ Falling	68	75	82	%
UVP Debounce Interval				5		μs

■ FUNCTION DESCRIPTION

Power-On-Reset (POR)

The UTC **LC1111** monitors the V_{CC} pin voltage (V_{CC}) for power-on-reset function to prevent wrong operation. The built-in POR circuit keeps the output shutting off until internal circuit is operating properly. Typical POR threshold is 4.0V with 0.4V hysteresis.

Soft-Start

The UTC **LC1111** provides an adjustable soft-start circuitry to control rise rate of the output voltage and limit the current surge during start-up. The soft-start time is set with a capacitor from the SS pin to the ground. The capacitor is charged to VP with a constant 4.5mA (typ.) current source.

Under-Voltage Protection (UVP)

The UTC **LC1111** monitors the voltage on FB. When the voltage on FB falls below the under-voltage threshold, the UVP circuit shuts off the output voltage immediately by pulling down DRV to 0V and latches UTC **LC1111** off, requiring either a V_{CC} POR or EN re-enable again to restart. The UTC **LC1111** UVP is activated after V_{OUT} voltage has reached 90% POK threshold while the UTC **LC1111** UVP is activated after V_{CC} has been applied to V_{CC} pin.

Enable Control

The UTC **LC1111** has a dedicated enable pin (EN). A logic low signal applied to this pin shuts down the output. Following a shutdown, a logic high signal re-enables the output through initiation of a new soft-start cycle. It's not necessary to use an external transistor to save cost.

Power-OK and Delay

The UTC **LC1111** indicates the status of the output voltage by monitoring the feedback voltage (V_{FB}) on FB pin. As the V_{FB} rises and reaches the rising Power-OK voltage threshold (V_{POKTH}), an internal delay function starts to work. At the end of the delay time, the IC turns off the internal NMOS of the POK to indicate that the output is ok. As the V_{FB} falls and reaches the falling Power-OK voltage threshold, the IC turns on the NMOS of the POK (after a debounce time of 5ms typical).

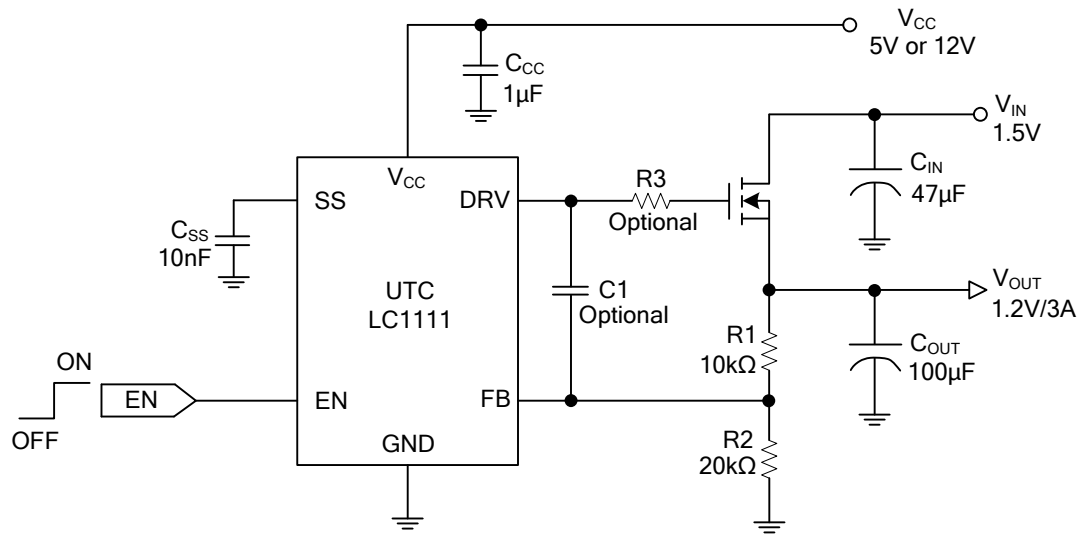
Output Voltage Regulation

The UTC **LC1111** is a linear regulator controller. An external N-channel MOSFET should be connected to DRV as the pass element. The output voltage set by the resistor divider is determined by:

$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R1}{R2}\right)$$

Where R1 is connected from V_{OUT} to FB and R2 is connected from FB to GND.

■ TYPICAL APPLICATION CIRCUIT



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