

UNISONIC TECHNOLOGIES CO., LTD

7N80-Q **Preliminary Power MOSFET**

7A, 800V N-CHANNEL POWER MOSFET

DESCRIPTION

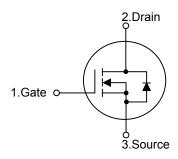
The UTC 7N80-Q is a N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology specialized in allowing a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC 7N80-Q is universally applied in high efficiency switch mode power supply.



- * $R_{DS(on)}$ < 1.8 Ω @ V_{GS} =10V, I_{D} =3.5A
- * Improved dv/dt capability
- * Fast switching
- * 100% avalanche tested

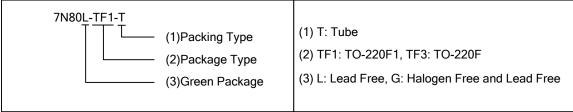
SYMBOL



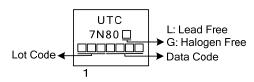
ORDERING INFORMATION

Ordering Number		Doolsons	Pin Assignment			Dooking	
Lead Free	Halogen Free	Package	1	2	3	Packing	
7N80L-TF1-T	7N80G-TF1-T	TO-220F1	G	D	S	Tube	
7N80L-TF3-T	7N80G-TF3-T	TO-220F	G	D	S	Tube	

Note: Pin Assignment: G: Gate D: Drain S: Source



MARKING



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TO-220F

TO-220F1

■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	800	V
Gate-Source Voltage		V_{GSS}	±30	V
Drain Current (Note 2)	Continuous	I_{D}	7	Α
	Pulsed	I_{DM}	28	Α
Avalanche Energy	Single Pulsed (Note 3)	E _{AS}	580	mJ
	Repetitive (Note 2)	E _{AR}	15.8	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	4.5	V/ns
Power Dissipation		P_{D}	51	W
Junction Temperature		T_J	+150	°C
Storage Temperature		T_{STG}	-55~+150	°C

- Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

 Absolute maximum ratings are stress ratings only and functional device operation is not implied.
 - 2. Repetitive Rating: Pulse width limited by maximum junction temperature.
 - 3. L = 24mH, I_{AS} = 7A, V_{DD} = 50V, R_G = 25 Ω , Starting T_J = 25 $^{\circ}$ C
 - 4. $I_{SD} \le 7A$, di/dt $\le 200A/\mu s$, $V_{DD} \le BV_{DSS}$, Starting $T_J = 25^{\circ}C$

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT	
Junction to Ambient	θ_{JA}	62.5	°C/W	
Junction to Case	$\theta_{ m JC}$	2.45	°C/W	

■ ELECTRICAL CHARACTERISTICS (T_c=25°C, unless otherwise specified)

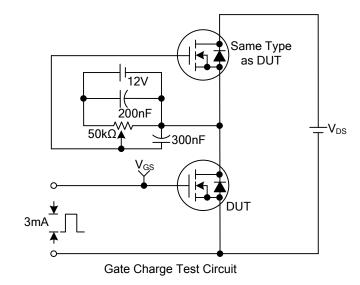
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PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	800			V
Breakdown Voltage Temperature Coefficient		$\triangle BV_{DSS}/\triangle T_{J}$	Reference to 25°C, I _D =250µA		0.97		V/°C
Drain-Source Leakage Current		I _{DSS}	V _{DS} =800V, V _{GS} =0V			10	
			V _{DS} =640V, T _C =125°C			100	μΑ
Gate- Source Leakage Current	Forward	I _{GSS}	V _{GS} =+30V, V _{DS} =0V			100	nA
	Reverse		V _{GS} =-30V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_{D}=250\mu A$			5.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =3.5A			1.8	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}			700		pF
Output Capacitance		Coss	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		110		pF
Reverse Transfer Capacitance		C _{RSS}	1		15		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q_{G}	V _{DS} =50V, I _D =1.3A		36		nC
Gate to Source Charge		Q_GS	V _{DS} =50V, I _D =1.3A I _q =100μA (Note 1, 2)		9		nC
Gate to Drain Charge		Q_GD	-1 _{1g} -100μΑ (Note 1, 2)		12		nC
Turn-ON Delay Time		t _{D(ON)}			75		ns
Rise Time		t _R	V _{DD} =400V, V _{GS} =10V, I _D =0.5A,		135		ns
Turn-OFF Delay Time		t _{D(OFF)}	R _G =25Ω (Note 1, 2)		195		ns
Fall-Time		t⊧			100		ns
SOURCE- DRAIN DIODE RATIN	GS AND CH	ARACTERISTI	CS				
Drain-Source Diode Forward Voltage		V_{SD}	I _S =7A, V _{GS} =0V			1.4	V
Maximum Body-Diode Continuous Current		Is				7	Α
Maximum Body-Diode Pulsed Current		I _{SM}				28	Α
Reverse Recovery Time		t _{rr}	I _S =7A, V _{GS} =0V,		615		ns
Reverse Recovery Charge		Q_{rr}	dI _F /dt=100A/μs (Note 1)		5.4		μC

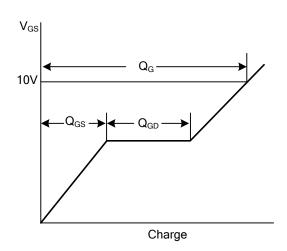
Notes: 1. Pulse Test: Pulse width ≤ 300µs, Duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

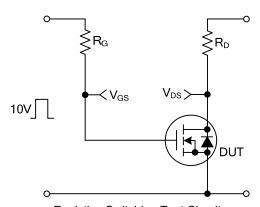


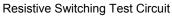
■ TEST CIRCUITS AND WAVEFORMS

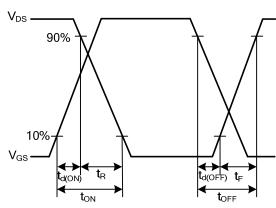




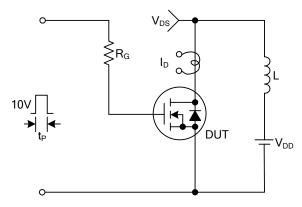
Gate Charge Waveforms



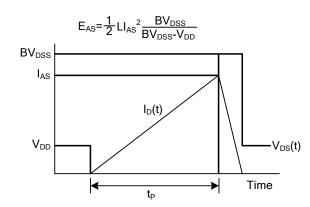




Resistive Switching Waveforms

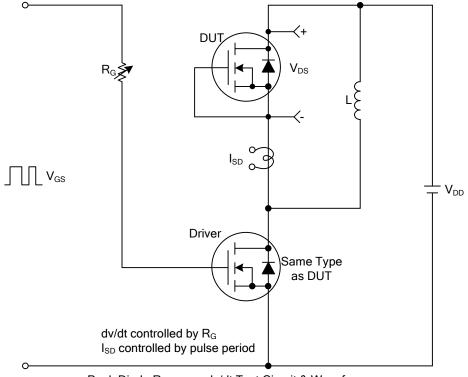


Unclamped Inductive Switching Test Circuit

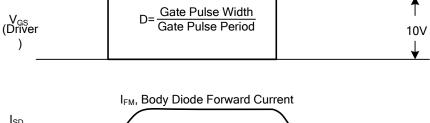


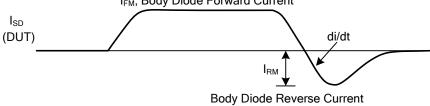
Unclamped Inductive Switching Waveforms

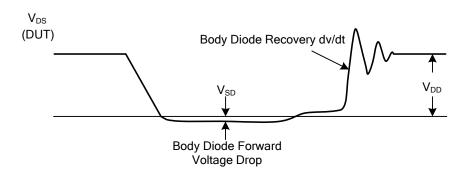
■ TEST CIRCUITS AND WAVEFORMS(Cont.)



Peak Diode Recovery dv/dt Test Circuit & Waveforms







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