



2N70-CA

Power MOSFET

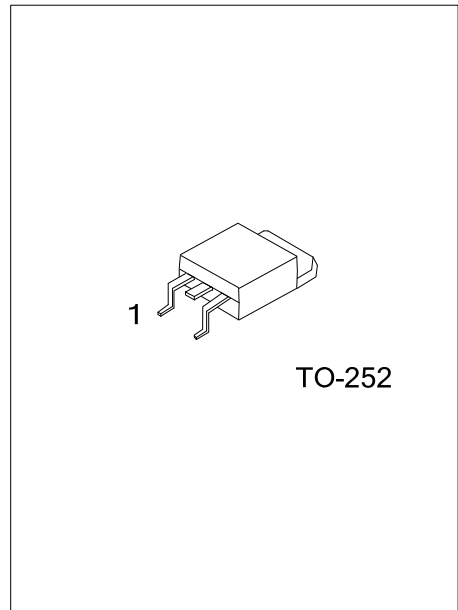
2A, 700V N-CHANNEL POWER MOSFET

DESCRIPTION

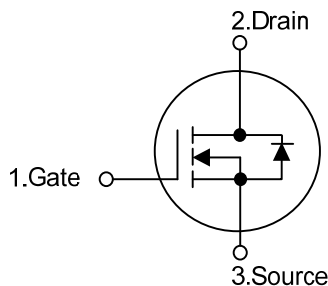
The UTC **2N70-CA** is a high voltage MOSFET designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and high rugged avalanche characteristics. This power MOSFET is usually used at high speed switching applications in power supplies, PWM motor controls, high efficient DC to DC converters and bridge circuits.

FEATURES

- * $R_{DS(ON)} < 5.2\Omega @ V_{GS} = 10V, I_D = 1.0 A$
- * Fast switching capability
- * Avalanche energy specified
- * Improved dv/dt capability, high ruggedness



SYMBOL



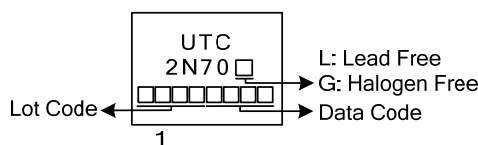
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
2N70L-TN3-R	2N70G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>2N70L-TN3-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) TN3: TO-252</p> <p>(3) L: Lead Free, G: Halogen Free and Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	700	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	2.0	A
	Pulsed (Note 2)	I_{DM}	8.0	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	100	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	4.5	V/ns
Power Dissipation		P_D	30	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Operating Temperature		T_{OPR}	-55 ~ +150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by T_J .

3. $L=40\text{mH}$, $I_{AS}=2.0\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\ \Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD}\leq 2.0\text{A}$, $di/dt\leq 200\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL RESISTANCES CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	110	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	4.24	$^\circ\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	700			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} = 700V, V _{GS} = 0V			10	μA
Gate-Source Leakage Current	Forward	I _{GSS}			100	nA
	Reverse				-100	nA
Breakdown Voltage Temperature Coefficient	ΔBV _{DSS} /ΔT _J	I _D = 250 μA, Referenced to 25°C		0.4		V/°C
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 250μA	3.0		5.0	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 1.0A			5.2	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz		240		pF
Output Capacitance	C _{OSS}			37		pF
Reverse Transfer Capacitance	C _{RSS}			3.7		pF
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	t _{D(ON)}	V _{DD} = 30V, I _D = 0.5A, R _G = 25Ω (Note 1, 2)		40		ns
Turn-On Rise Time	t _R			24		ns
Turn-Off Delay Time	t _{D(OFF)}			65		ns
Turn-Off Fall Time	t _F			19		ns
Total Gate Charge	Q _G	V _{DS} = 50V, I _D = 1.3A, V _{GS} = 10V (Note 1, 2)		12		nC
Gate-Source Charge	Q _{GS}			4.7		nC
Gate-Drain Charge	Q _{GD}			1.8		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
Drain-Source Diode Forward Voltage	V _{SD}	V _{GS} = 0 V, I _{SD} = 2.0 A			1.4	V
Continuous Drain-Source Current	I _{SD}				2.0	A
Pulsed Drain-Source Current	I _{SM}				8.0	A
Body Diode Reverse Recovery Time	t _{RR}	I _S = 2.0A, di/dt = 100A/μs		300		nS
Body Diode Reverse Recovery Charge	Q _{RR}			1.3		nC

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%

2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

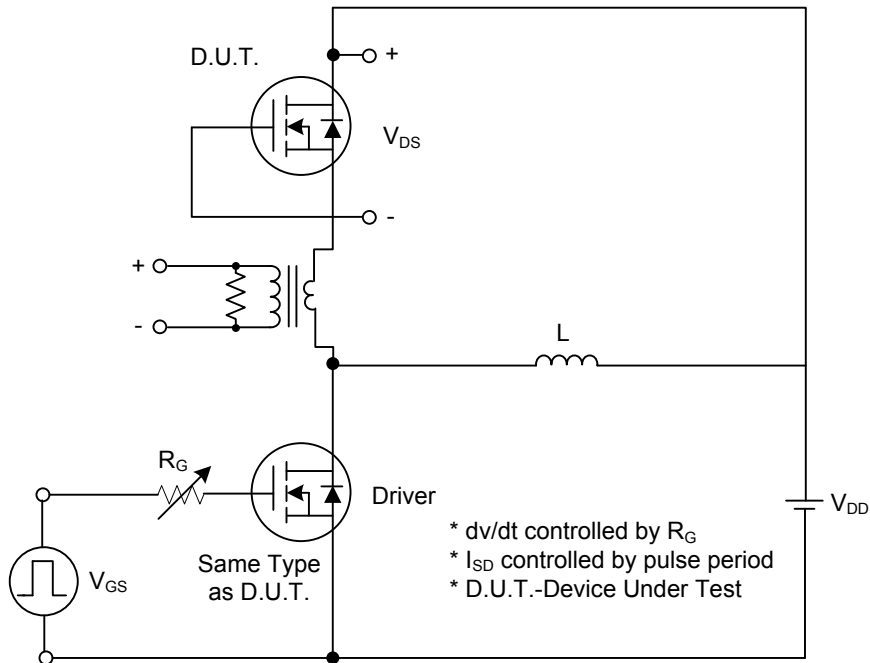


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

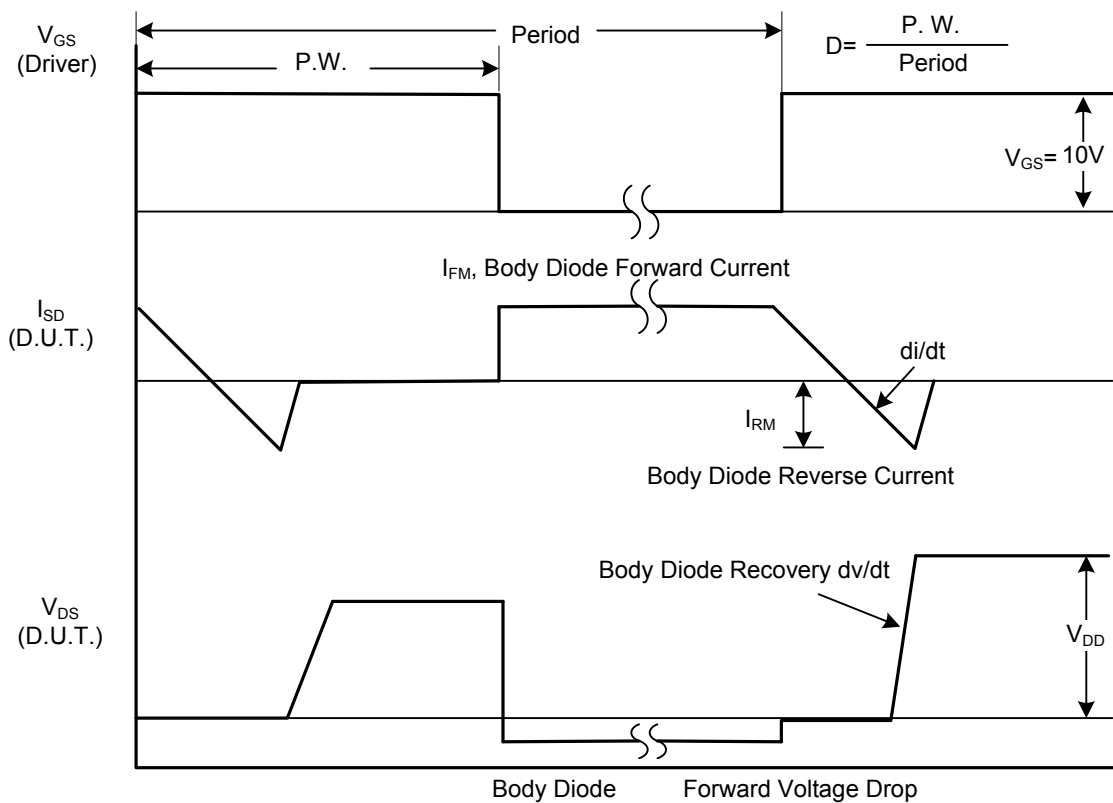


Fig. 1B Peak Diode Recovery dv/dt Waveforms

TEST CIRCUITS AND WAVEFORMS (Cont.)

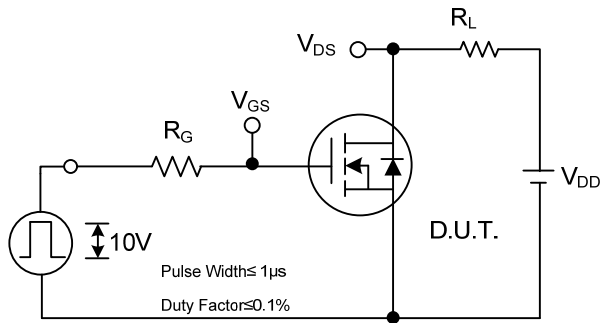


Fig. 2A Switching Test Circuit

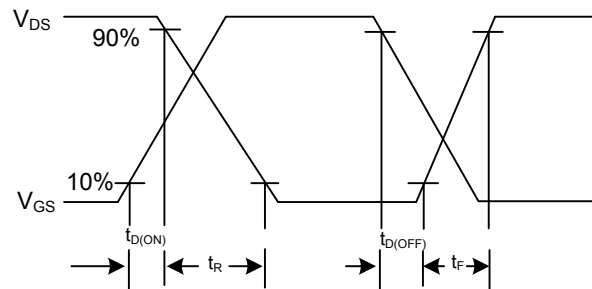


Fig. 2B Switching Waveforms

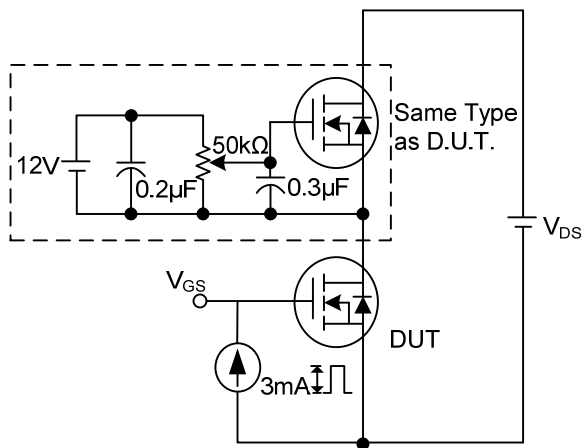


Fig. 3A Gate Charge Test Circuit

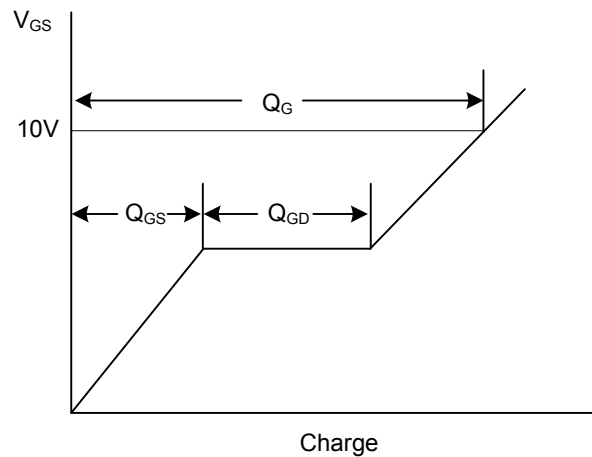


Fig. 3B Gate Charge Waveform

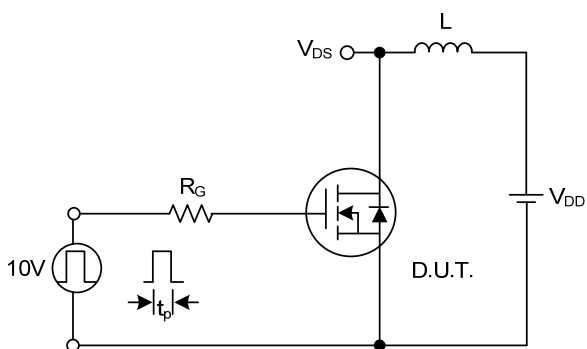


Fig. 4A Unclamped Inductive Switching Test Circuit

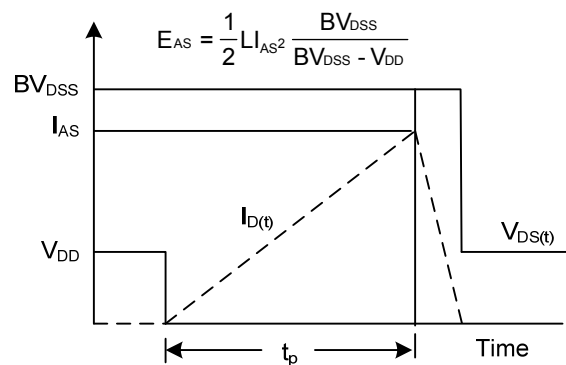
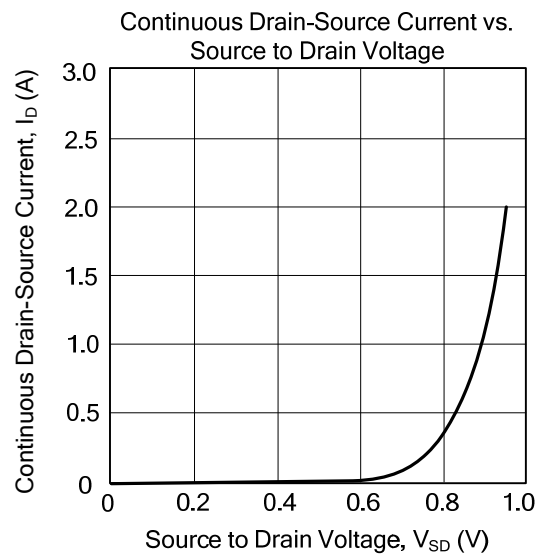
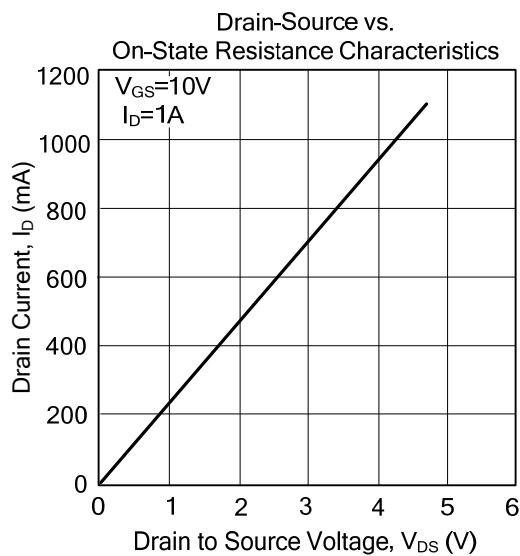
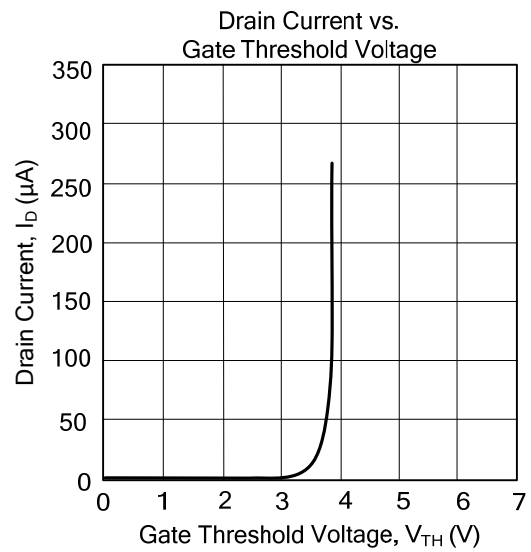
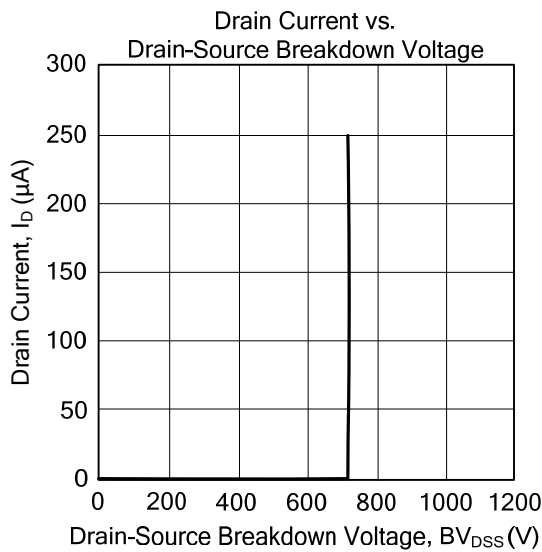


Fig. 4B Unclamped Inductive Switching Waveforms

TYPICAL CHARACTERISTICS



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