



4N90-KA

Advance

Power MOSFET

4 Amps, 900 Volts N-CHANNEL POWER MOSFET

DESCRIPTION

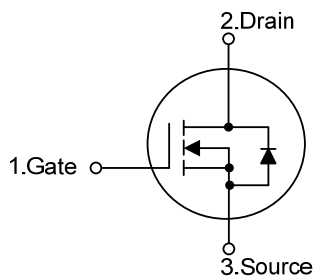
The UTC **4N90-KA** is a N-channel enhancement MOSFET adopting UTC's advanced technology to provide customers with DMOS, planar stripe technology. This technology is designed to meet the requirements of the minimum on-state resistance and perfect switching performance. It also can withstand high energy pulse in the avalanche and communication mode.

The UTC **4N90-KA** is particularly applied in high efficiency switch mode power supplies.

FEATURES

- * $R_{DS(ON)} < 4.2\Omega @ V_{GS}=10V, I_D=2A$
- * High switching speed
- * 100% avalanche tested
- * Improved dv/dt capability

SYMBOL



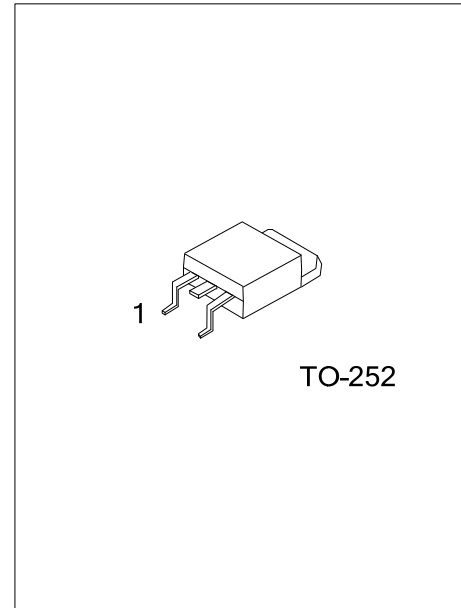
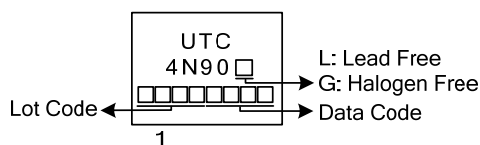
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
4N90L-TN3-R	4N90G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>4N90L-TN3-T</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) R: Tape Reel (2) TN3: TO-252 (3) L: Lead Free, G: Halogen Free and Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain to Source Voltage	V_{DSS}	900	V
Gate to Source Voltage	V_{GSS}	± 30	V
Avalanche Current (Note 2)	I_{AR}	4	A
Continuous Drain Current	Continuous	I_D	4
	Pulsed (Note 2)	I_{DM}	16
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	240
	Repetitive (Note 2)	E_{AR}	14
Peak Diode Recovery dv/dt (Note 4)	dv/dt	4.5	V/ns
Power Dissipation ($T_C=25^\circ\text{C}$)	P_D	54	W
Derate above 25°C		0.43	W/ $^\circ\text{C}$
Operating Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature

3. $L=30\text{mH}$, $I_{AS}=4\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$

4. $I_{SD}\leq 4\text{A}$, $di/dt\leq 200\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$

■ THERMAL RESISTANCES CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	110	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	2.3	$^\circ\text{C}/\text{W}$

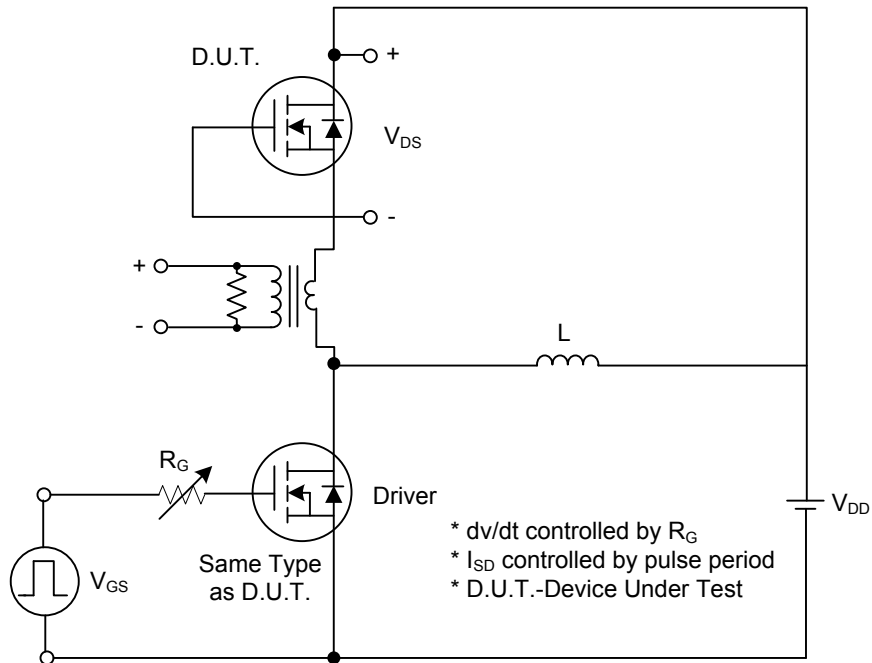
■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
OFF CHARACTERISTICS								
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D =250μA	900			V	
Breakdown Voltage Temperature Coefficient		ΔBV _{DSS} /ΔT _J	I _D =250μA, Referenced to 25°C		1.05		V/°C	
Drain-Source Leakage Current		I _{DSS}	V _{DS} =900V, V _{GS} =0V			10	μA	
			V _{DS} =720V, T _C =125°C			100	μA	
Gate- Source Leakage Current	Forward	I _{GSS}	V _{GS} =+30V, V _{DS} =0V			+100	nA	
	Reverse	I _{GSS}	V _{GS} =-30V, V _{DS} =0V			-100	nA	
ON CHARACTERISTICS								
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	3.0		5.0	V	
Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =2A		3.5	4.2	Ω	
DYNAMIC PARAMETERS								
Input Capacitance		C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz		900		pF	
Output Capacitance		C _{OSS}				67		pF
Reverse Transfer Capacitance		C _{RSS}				50		pF
SWITCHING PARAMETERS								
Total Gate Charge		Q _G	V _{DS} =50V, V _{GS} =10V, I _D =1.3A (Note 1,2)		38		nC	
Gate-Source Charge		Q _{GS}				7.5		nC
Gate-Drain Charge		Q _{GD}				8.8		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =30V, I _D =0.5A, R _G =25Ω (Note 1,2)		65		ns	
Turn-ON Rise Time		t _R				56		ns
Turn-OFF Delay Time		t _{D(OFF)}				130		ns
Turn-OFF Fall Time		t _F				50		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS								
Maximum Body-Diode Continuous Current		I _S				4	A	
Maximum Body-Diode Pulsed Current		I _{SM}				16	A	
Drain-Source Diode Forward Voltage		V _{SD}	I _S =4A, V _{GS} =0V			1.4	V	

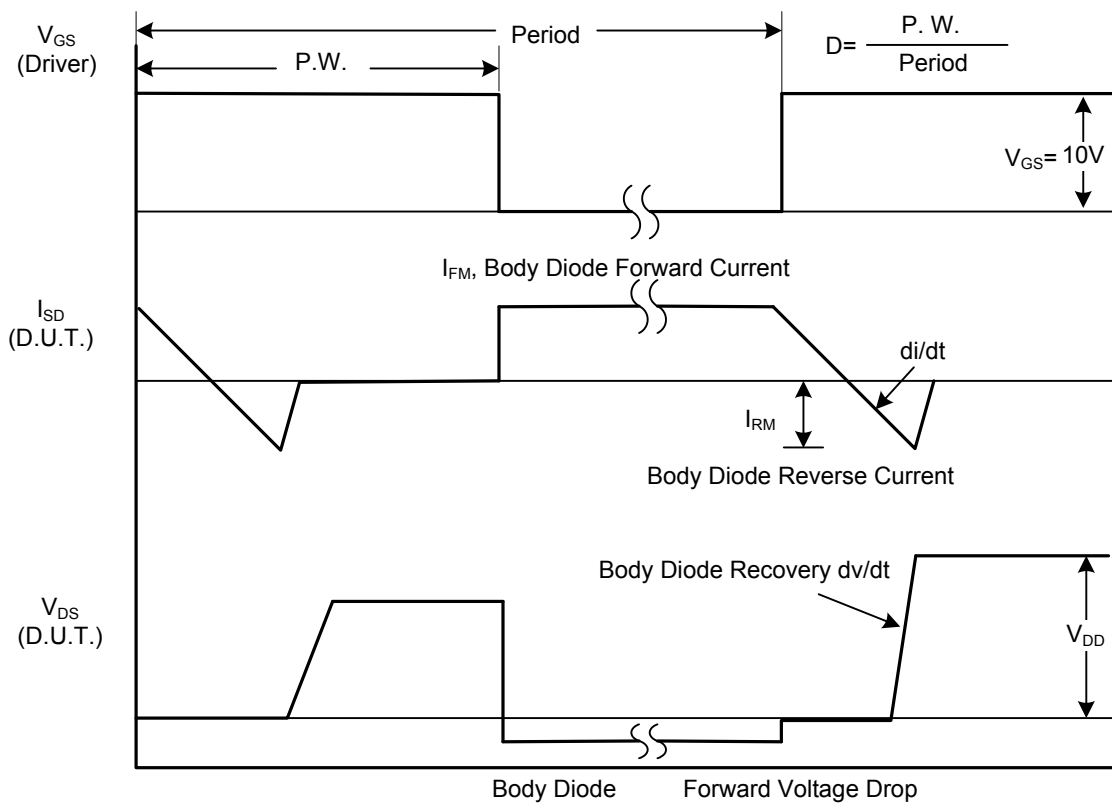
Notes: 1. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

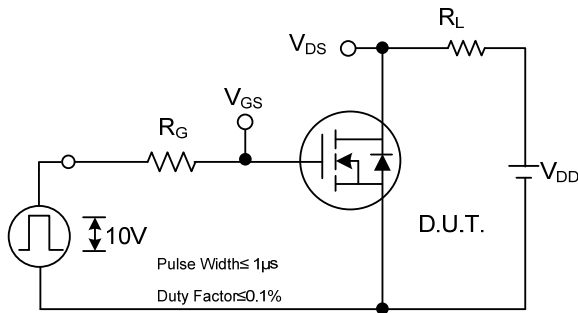


Peak Diode Recovery dv/dt Test Circuit

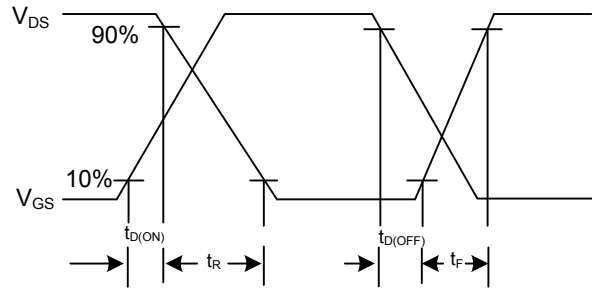


Peak Diode Recovery dv/dt Waveforms

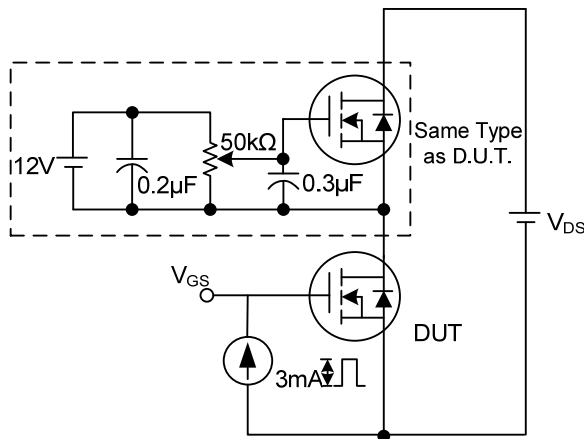
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



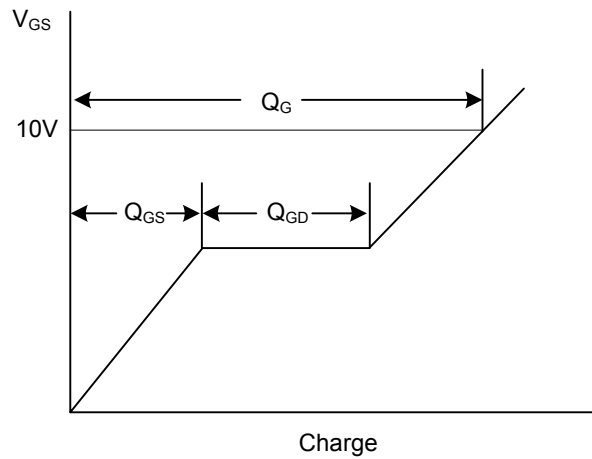
Switching Test Circuit



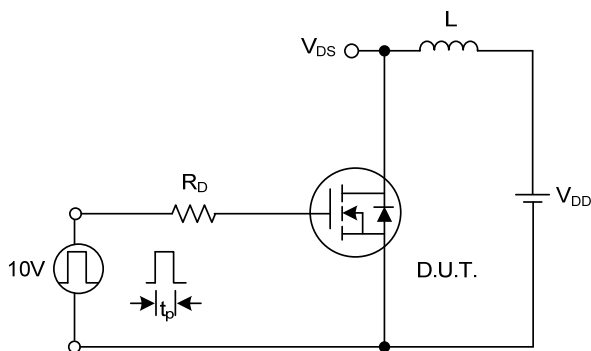
Switching Waveforms



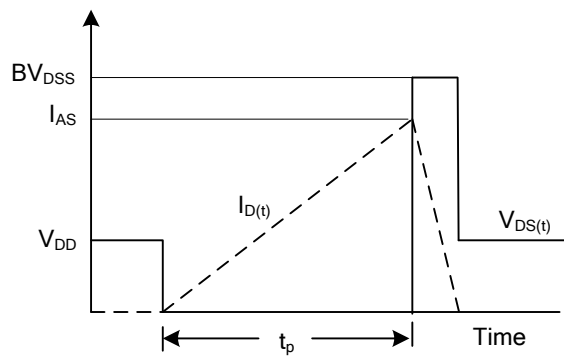
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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