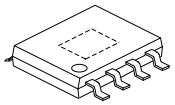
1.5A, LOW DROPOUT REGULATOR WITH POWER GOOD



HSOP-8

■ DESCRIPTION

The **UTC LR1965** is CMOS-based positive voltage and a very low dropout regulator IC that minimum input voltage is 2.5V and is capable of delivering the continuous output load current up to 1.5A.

It has features of low dropout (maximum 300mV at 1A), a very low quiescent current (typically 300uA at 0.1A) and very high PSRR up to 86dB at 1A load current.

The output voltage can be set from 0.8V to (V_{IN} - V_{DRP}) with an external resistor divider and it has ±2% accuracy through all temperature ranges include the line as well as load variations. It is allowed to use a small 4.7μF MLCC input and output capacitor to deliver the current with the stable operation.

Built-in Soft-Start function reduces the inrush current and the other features are include over current protection (OCP), short-circuit protection (SCP), and thermal shut down protection (TSD).

The **UTC LR1965** is available in 8-SOP-EP package with exposed pad for optimal power dissipation and 8-TDFN (3x3mm).

■ FEATURES

* Input Voltage Range: 2.5V~6.0V
* Supply Current .: Typ. 300uA
* Current limit : Min. 1.8A
* Adjustable Output from 0.8V
* LR1965: Typ 0.4V Dropout @ I_{OUT}=1.5A
* Compatible with MLCC Capacitors
* Built-in Soft-Start Limits Inrush Current
* Built-in Thermal Shutdown Protection
* Built-in Over Current & Short Circuit Protection

■ ORDERING INFORMATION

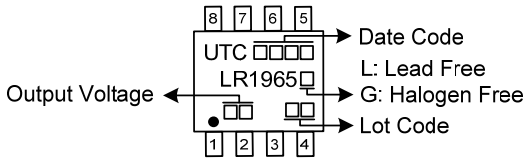
Ordering Number		Package	Packing
Lead Free	Halogen Free		
LR1965L-xx-SH2-R	LR1965G-xx-SH2-R	HSOP-8	Tape Reel

Note: xx: Output Voltage, refer to Marking Information.

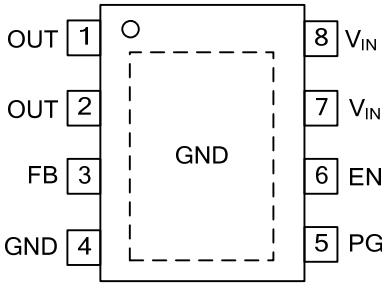
LR1965G-xx-SH2-R

(1)Packing Type	(1) R: Tape Reel
(2)Package Type	(2) SH2: HSOP-8
(3)Output Voltage Code	(3) xx: refer to Marking Information
(4)Green Package	(4) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING INFORMATION

PACKAGE	VOLTAGE CODE	MARKING
HSOP-8	AD: ADJ	

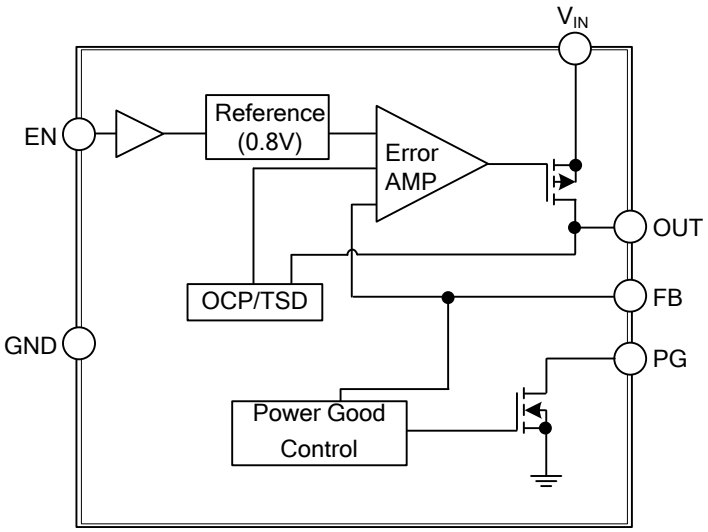
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1, 2	OUT	Voltage Regulator Output Pin
3	FB	Feedback Pin. Connect to output through a voltage-divider to set the output. Recommended that the tolerance of feedback resistors is below 1%.
4	GND	Ground Pin
5	PG	Open Drain Power-Good (PG) Output.
6	EN	Chip Enable Pin
7, 8	V_{IN}	Input Supply Voltage Pin.
Exposed Pad	GND	Connect exposed pad to GND.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage	V_{IN}	-0.3 ~ 7	V
Output Voltage	OUT	-0.3 ~ V_{IN}+0.3	V
Junction to Ambient	θ_{JA}	50	°C/W
Junction to Case	θ_{JC}	10	°C/W
Junction Temperature	T_J	+150	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage Range	V_{IN}	2.5 ~ 6.0	V
Ambient Temperature Range	T_A	-40 ~ +85	°C

■ ELECTRICAL CHARACTERISTICS

All parameters are guaranteed over the operational supply voltage and temperature range. Operating conditions unless otherwise noted are: V_{IN}=5V, OUT=2.5V and T_A=25°C. Typical values are for information only.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage						
Quiescent Current	I_Q	I_{OUT}=100mA		300		uA
Shutdown Current	I_{STD}	V_{IN}=6V, V_{EN}=GND		0.2	2	uA
Feedback (FB)						
Feedback Voltage Accuracy	V_F	I_{OUT}=10mA, T_A =25°C	784	800	816	mV
Input Bias Current	I_F	V_{FB}=0.8V, V_{IN} =6V		0.001	0.1	uA
Output (OUT)						
Output Accuracy	V_{OUT}		-2		2	%
Load Regulation	R_{LO}	I_{OUT}=1mA to 1.5A		0.1	2	%/A
Line Regulation	R_{LN}	V_{IN}=2.2~6V, V_{OUT}=1.225V, I_{OUT}=1mA	-0.2		0.2	%/V
Dropout Voltage	V_{DRP}	I_{OUT}=1.5A,V_{FB}=768mV		400		mV
		I_{OUT}=1A,V_{FB}=768mV		140	280	
		I_{OUT}=0.5A,V_{FB}=768mV			200	
Current Limit	I_C		1.8			A
Load transient (Note 1)	L_{OT}	I_{OUT}=20mA to 1.5A,		3		%
Line Transient (Note 1)	R_{NT}	ΔV_{IN}=0.5V		3		%
Enable (EN))						
Input Threshold	V_{ENH}	EN rising, V_{IN}=OUT+1V~6V	1.2			V
	V_{ENL}	EN falling, V_{IN}=OUT+1V~6V			0.4	
Input Bias Current	I_{EN}	EN=0 or 6V	-1	0	1	uA
Power Good (PG)						
Threshold Voltage	P_{V1}	FB high, V_{HYS}=10mV, V_{IN}=OUT+1V~6V	835	880	924	mV
	P_{V2}	FB low, V_{HYS}=10mV, V_{IN}=OUT+1V~6V	652	688	760	mV
Output Voltage Low	P_{CL}	FB=0.6V or 1.0V, I_{PG}=1mA		25	200	mV
Output Current High	P_{CH}	P_{WRGD}=6V		0.001	0.1	uA
Rising Delay Time	P_{RDT}	From FB*90% to PG		150		us
Falling Delay Time 1	P_{FDT1}	V_{IN}=2.5V, From FB to PG	20	70	120	us
Falling Delay Time 2	P_{FDT2}	V_{IN}=6V, From FB to PG	60	180	300	us
Thermal Shutdown (TSD) (Note 1)						
TSD Threshold	T_{SDON}	TSD On		165		°C
	T_{SDOFF}	TSD Off		145		°C

Note: Guaranteed by design but not production tested.

■ TYPICAL APPLICATION CIRCUIT