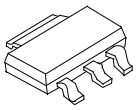
2.5A, 100V N-CHANNEL LOGIC LEVEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR



1

SOT-223

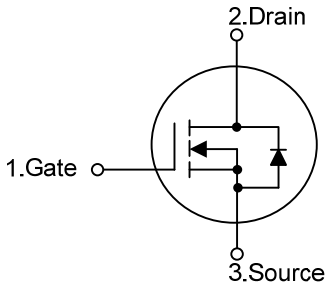
■ DESCRIPTION

The UTC **UTT3N10-H** is an N-channel logic level enhancement mode field effect transistor, it uses UTC's advanced technology to provide the customers with high switching speed and low gate charge.

■ FEATURES

* $R_{DS(on)}$ < 225mΩ @ V_{GS} = 10V, I_D = 1.25A
  $R_{DS(on)}$ < 360mΩ @ V_{GS} = 4.5V, I_D = 125A
* High switching speed
* Low grage

■ SYMBOL



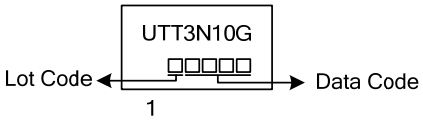
■ ORDERING INFORMATION

Order Number	Package	Pin Assignment			Packing
		1	2	3	
UTT3N10G-AA3-R	SOT-223	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UTT3N10G-AA3-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) AA3: SOT-223 (3) G: Halogen Free and Lead Free

■ MARKING



■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C, unless otherwise noted)

PARAMETER			SYMBOL	RATINGS	UNIT
Drain-Source Voltage			V_{DSS}	+100	V
Gate-Source Voltage			V_{GSS}	±20	V
Drain Current	Continuous (Note 1)	T_A=25°C	I_D	2.5	A
		T_A=70°C		2.0	A
	Pulsed (Note 2)		I_{DM}	10	A
Single Pulsed Avalanche Energy			E_{AS}	12	mJ
Power Dissipation (Note 1)	T_A=25°C		P_D	3	W
	T_A=70°C			1.9	
Junction Temperature			T_J	-55~+150	°C
Storage Temperature Range			T_{STG}	-55~+150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL CHARACTERISTICS

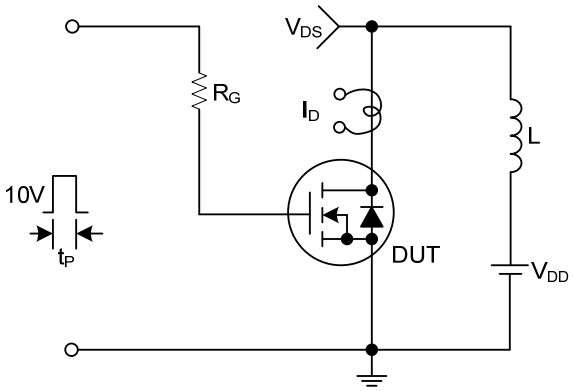
PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Case (Note 1)	θ_{JC}	12	°C/W
Junction to Ambient (Note 1)	θ_{JA}	42	°C/W

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise noted)

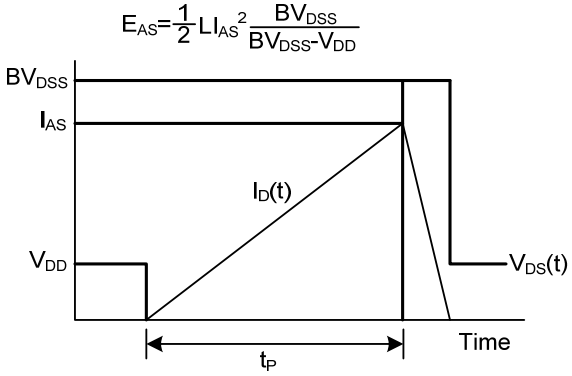
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	I_D=250μA, V_{GS}=0V	100			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=80V, V_{GS}=0V			1	μA
Gate-Source Leakage Current	Forward	I_{GSS}	V_{GS}=+20V, V_{DS}=0V			+100	nA
	Reverse		V_{GS}=-20V, V_{DS}=0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	1	1.6	2.5	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=1.25A		180	225	mΩ
			V_{GS}=4.5V, I_D=1A		265	360	mΩ
Forward Transconductance		g_{FS}	V_{DS}=20V, I_D=1.25A		2.3		S
DYNAMIC PARAMETERS (Note 3)							
Input Capacitance		C_{ISS}	V_{GS}=0V, V_{DS}=25V, f=1.0MHz		550		pF
Output Capacitance		C_{OSS}			30		pF
Reverse Transfer Capacitance		C_{RSS}			19		pF
SWITCHING PARAMETERS (Note 3)							
Total Gate Charge		Q_G	V_{GS}=10V, V_{DS}=50V, I_D=1.3A I_G=100μA		65		nC
Gate to Source Charge		Q_{GS}			2.5		nC
Gate to Drain Charge		Q_{GD}			2.2		nC
Turn-ON Delay Time		$t_{D(ON)}$	V_{DD}=30V, I_D=0.5A, R_G=25Ω, V_{GS}=10V		25		ns
Rise Time		t_R			12		ns
Turn-OFF Delay Time		$t_{D(OFF)}$			150		ns
Fall-Time		t_F			55		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Drain-Source Diode Forward Voltage		V_{SD}	I_S=1A, V_{GS}=0V		0.8	1.2	V

Note: 1. Surface Mounted on FR4 Board, t ≤10sec.
2. Pulse Test: Pulse Width ≤ 300us, Duty Cycle ≤ 2%
3. Guaranteed by design, not subject to production testing
4. Starting T_J=25°C, L=0.5mH, V_{DD}=50V

■ TEST CIRCUITS AND WAVEFORMS



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms