



UTT1D5N10

Power MOSFET

1.5A, 100V N-CHANNEL LOGIC LEVEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

DESCRIPTION

The UTC **UTT1D5N10** is an N-channel MOSFET, it uses UTC's advanced technology to provide the customers with high switch speed and low gate charge.

FEATURES

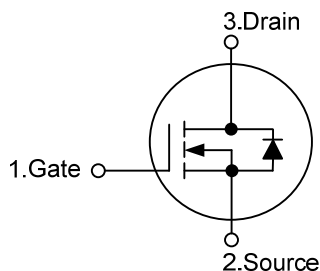
* $R_{DS(ON)} \leq 280 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=0.75\text{A}$

$R_{DS(ON)} \leq 300 \text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$, $I_D=0.7\text{A}$

* High switch speed

* Low gate charge

SYMBOL



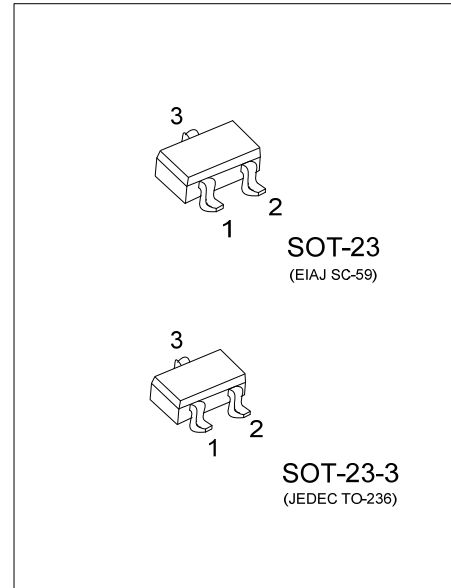
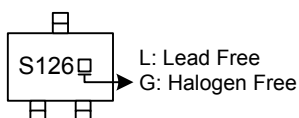
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UTT1D5N10L-AE2-R	UTT1D5N10G-AE2-R	SOT-23-3	G	S	D	Tape Reel
UTT1D5N10L-AE3-R	UTT1D5N10G-AE3-R	SOT-23	G	S	D	Tape Reel

Note: Pin Assignment: G: Gate S: Source D: Drain

UTT1D5N10G-AE2-R	(1)Packing Type	(1) R: Tape Reel
	(2)Package Type	(2) AE2: SOT-23-3, AE3: SOT-23
	(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT	
Drain-Source Voltage		V_{DSS}	100	V	
Gate-Source Voltage		V_{GSS}	± 20	V	
Drain Current	Continuous (Note 1)	I_D	$T_A=25^\circ\text{C}$	1.5	A
			$T_A=70^\circ\text{C}$	1.2	A
	Pulsed (Note 2)	I_{DM}		5	A
Power Dissipation (Note 1)	SOT-23	P_D		1.2	W
	SOT-23-3			1.1	W
Junction Temperature		T_J	-55 ~ +150	$^\circ\text{C}$	
Storage Temperature Range		T_{STG}	-55 ~ +150	$^\circ\text{C}$	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOT-23	θ_{JA}	104	$^\circ\text{C/W}$
Junction to Ambient	SOT-23-3	θ_{JA}	113	$^\circ\text{C/W}$

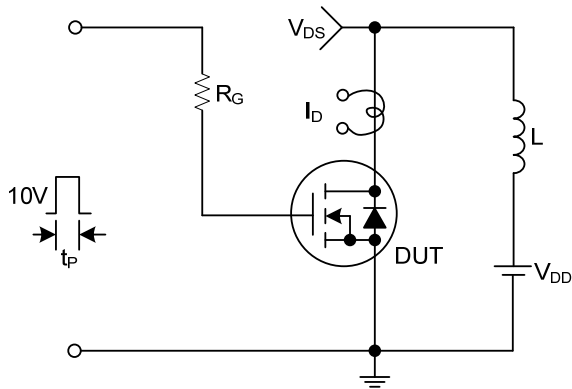
Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

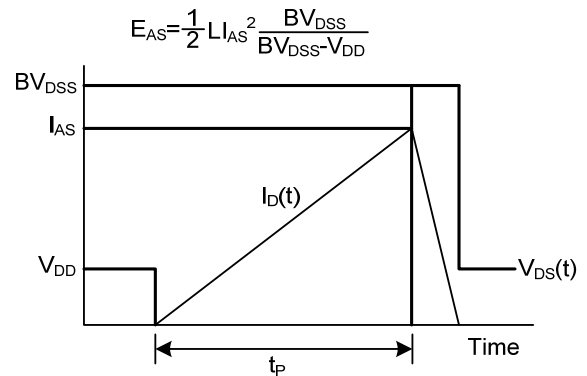
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	100			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=80\text{V}$, $V_{GS}=0\text{V}$			1	μA
Gate-Source Leakage Current	Forward	$V_{GS}=+20\text{V}$, $V_{DS}=0\text{V}$			+100	nA
	Reverse	$V_{GS}=-20\text{V}$, $V_{DS}=0\text{V}$			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.0	1.7	2.5	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=0.75\text{A}$			280	m Ω
		$V_{GS}=4.5\text{V}$, $I_D=0.7\text{A}$			300	m Ω
DYNAMIC PARAMETERS (Note 3)						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		420		pF
Output Capacitance	C_{OSS}			31		pF
Reverse Transfer Capacitance	C_{RSS}			21		pF
SWITCHING PARAMETERS (Note 3)						
Total Gate Charge	Q_G	$V_{DS}=80\text{V}$, $V_{GS}=10\text{V}$, $I_D=1.5\text{A}$		21		nC
Gate to Source Charge	Q_{GS}			3.5		nC
Gate to Drain Charge	Q_{GD}			2.7		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=50\text{V}$, $V_{GS}=10\text{V}$, $I_D=1.5\text{A}$, $R_G=25\Omega$		4.8		ns
Rise Time	t_R			16.5		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			42		ns
Fall-Time	t_F			28		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				1	A
Maximum Body-Diode Pulsed Current (Note 1)	I_{SM}				2	A
Drain-Source Diode Forward Voltage	V_{SD}	$I_S=1.5\text{A}$, $V_{GS}=0\text{V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_S=1.5\text{A}$, $V_{GS}=0\text{V}$,		43		ns
Body Diode Reverse Recovery Charge	Q_{rr}	$dI_F/dt=100\text{A}/\mu\text{s}$		30		nC

- Notes: 1. Surface Mounted on FR4 Board, $t \leq 10\text{sec}$.
 2. Pulse Test:Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
 3. Guaranteed by design, not subject to production testing.
 4. Starting $T_J=25^\circ\text{C}$, $L=0.5\text{mH}$, $V_{DD}=50\text{V}$.(See Figure1)

■ TEST CIRCUITS AND WAVEFORMS



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

Figure 1.

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