



## UT7852

Preliminary

Power MOSFET

### N-CHANNEL 80V (D-S) MOSFET

#### DESCRIPTION

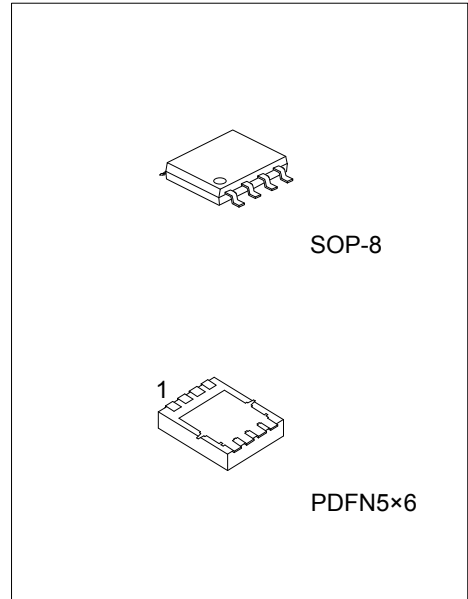
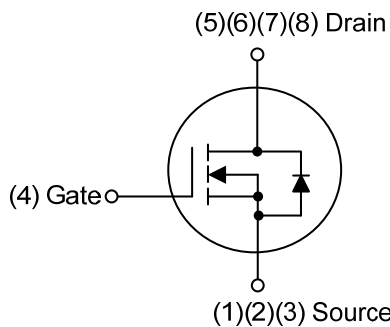
The UTC **UT7852** is an N-Channel MOSFET, it uses UTC's advanced technology to provide customers with a minimum on-state resistance and high switching speed.

The UTC **UT7852** is suitable for primary side switch for DC/DC applications.

#### FEATURES

- \* High switching speed
- \* Low on-state resistance

#### SYMBOL



#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT7852L-S08-R	UT7852G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel
UT7852L-P5060-R	UT7852G-P5060-R	PDFN5x6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UT7852G-S08-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) S08: UT7852, P5060: PDFN5x6</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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#### MARKING

SOP-8	PDFN5x6
<p>Date Code</p> <p>L: Lead Free</p> <p>G: Halogen Free</p> <p>Lot Code</p>	<p>Lot Code</p> <p>Date Code</p>

■ ABSOLUTE MAXIMUM RATINGS ( $T_A=25^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{DSS}$	80	V
Gate-Source Voltage		$V_{GSS}$	$\pm 20$	V
Pulsed Drain Current		$I_{DM}$	50	A
Continuous Drain Current ( $T_J=150^{\circ}\text{C}$ )(Note 1)	$T_A=25^{\circ}\text{C}$	$I_D$	12.5	A
	$T_A=70^{\circ}\text{C}$		10.0	A
Avalanche Current		$I_{AS}$	40	A
Continuous Source Current (Diode Conduction) (Note 1)		$I_S$	4.7	A
Power Dissipation (Note 1)	$T_A=25^{\circ}\text{C}$	SOP-8	1.5	W
		PDFN5x6	5.2	W
Junction Temperature		$T_J$	-55 ~ +150	$^{\circ}\text{C}$
Storage Temperature Range		$T_{STG}$	-55 ~ +150	$^{\circ}\text{C}$
Soldering Recommendations (Peak Temperature)			260	$^{\circ}\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL CHARACTERISTICS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Junction to Ambient (Note 1)	SOP-8	$\theta_{JA}$			85	$^{\circ}\text{C}/\text{W}$
	PDFN5x6			52	65	$^{\circ}\text{C}/\text{W}$
Junction to Case (Drain)	SOP-8	$\theta_{JC}$			24	$^{\circ}\text{C}/\text{W}$
	PDFN5x6			1.5	1.8	$^{\circ}\text{C}/\text{W}$

Note: Surface Mounted on 1" x 1" FR4 board.

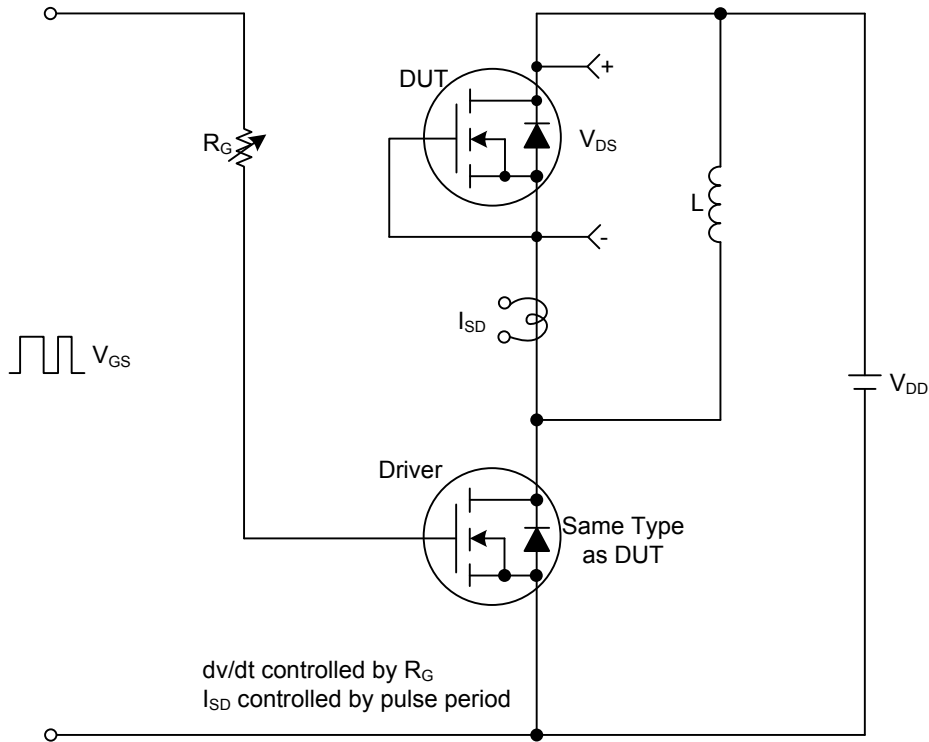
■ ELECTRICAL CHARACTERISTICS ( $T_J=25^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>							
Zero Gate Voltage Drain Current		$I_{DSS}$	$V_{DS}=80\text{V}, V_{GS}=0\text{V}$			1	$\mu\text{A}$
			$V_{DS}=80\text{V}, V_{GS}=0\text{V}, T_J=55^{\circ}\text{C}$			5	$\mu\text{A}$
Gate-Source Leakage Current	Forward	$I_{GSS}$	$V_{GS}=+20\text{V}, V_{DS}=0\text{V}$			+100	nA
	Reverse		$V_{GS}=-20\text{V}, V_{DS}=0\text{V}$			-100	nA
<b>ON CHARACTERISTICS</b>							
Gate Threshold Voltage		$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2.0			V
Static Drain-Source On-State Resistance (Note 1)		$R_{DS(ON)}$	$V_{GS}=10\text{V}, I_D=10\text{A}$		12.5	16.5	m $\Omega$
			$V_{GS}=6.0\text{V}, I_D=8.0\text{A}$		14	22	m $\Omega$
Forward Transconductance (Note 1)		$g_{FS}$	$V_{DS}=15\text{V}, I_D=10\text{A}$		25		S
On State Drain Current (Note 1)		$I_{D(ON)}$	$V_{DS}\geq 5\text{V}, V_{GS}=10\text{V}$	50			A
<b>DYNAMIC PARAMETERS (Note 2)</b>							
Gate Resistance		$R_G$			2		$\Omega$
<b>SWITCHING PARAMETERS</b>							
Total Gate Charge		$Q_G$	$V_{GS}=10\text{V}, V_{DS}=40\text{V}, I_D=10\text{A}$		34	41	nC
Gate to Source Charge		$Q_{GS}$			7.5		nC
Gate to Drain Charge		$Q_{GD}$			11.0		nC
Turn-ON Delay Time		$t_{D(ON)}$	$V_{DD}=30\text{V}, R_L=60\Omega, I_D\approx 0.5\text{A}, V_{GEN}=10\text{V}, R_G=25\Omega$		120		ns
Rise Time		$t_R$			130		ns
Turn-OFF Delay Time		$t_{D(OFF)}$			700		ns
Fall-Time		$t_F$			220		ns
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>							
Diode Forward Voltage (Note 1)		$V_{SD}$	$I_S=2.8\text{A}, V_{GS}=0\text{V}$		0.75	1.1	V
Source-Drain Reverse Recovery Time		$t_{rr}$	$I_F=2.8\text{A}, dI/dt=100\text{A}/\mu\text{s}$		45	75	ns

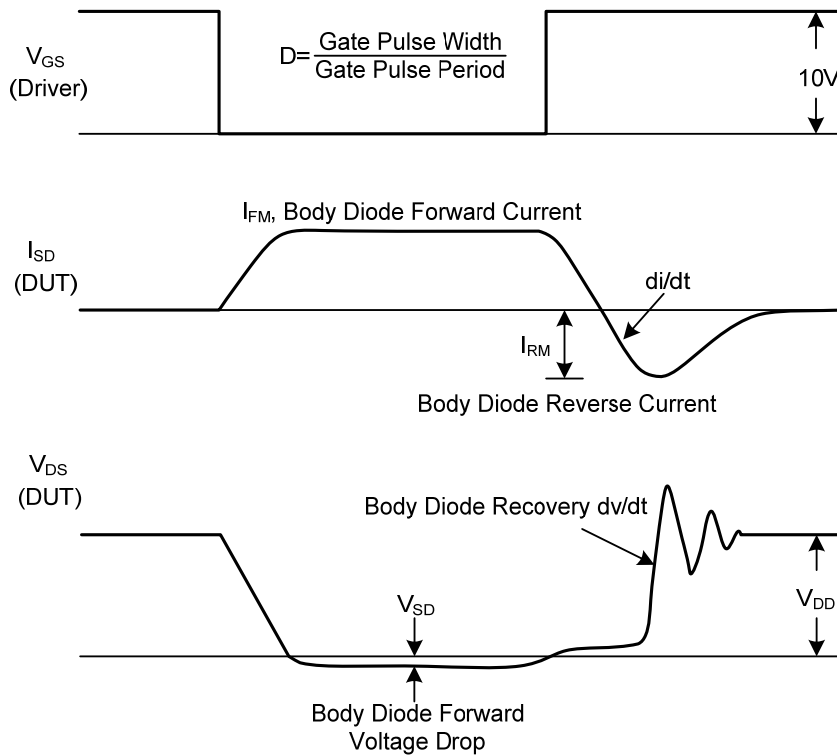
Notes: 1. Pulse test: pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .

2. Guaranteed by design, not subject to production testing.

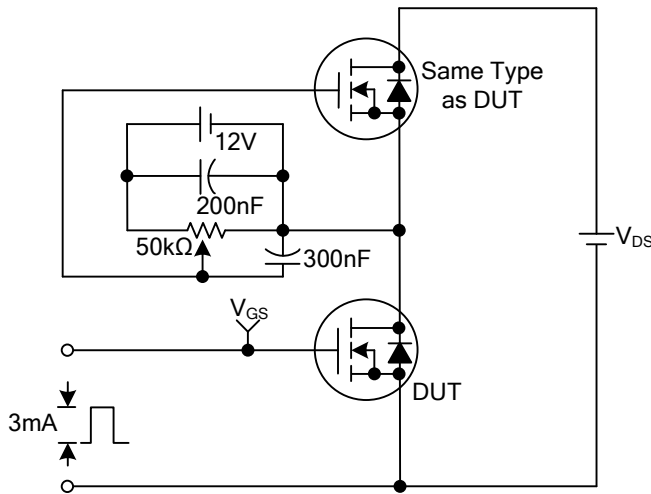
■ TEST CIRCUITS AND WAVEFORMS



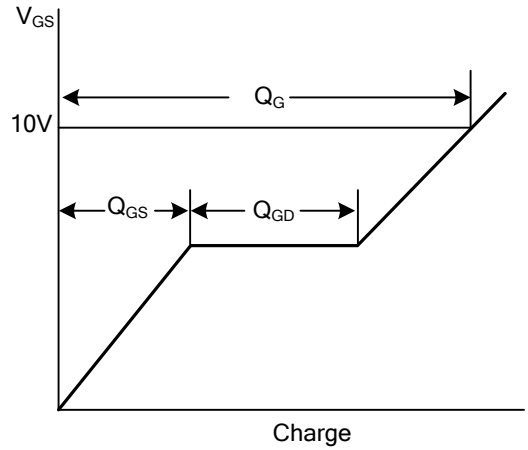
Peak Diode Recovery dv/dt Test Circuit & Waveforms



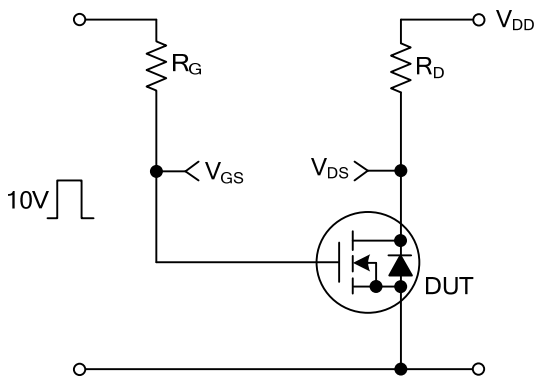
■ TEST CIRCUITS AND WAVEFORMS



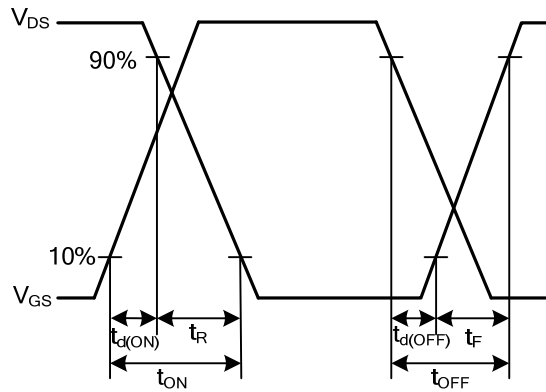
Gate Charge Test Circuit



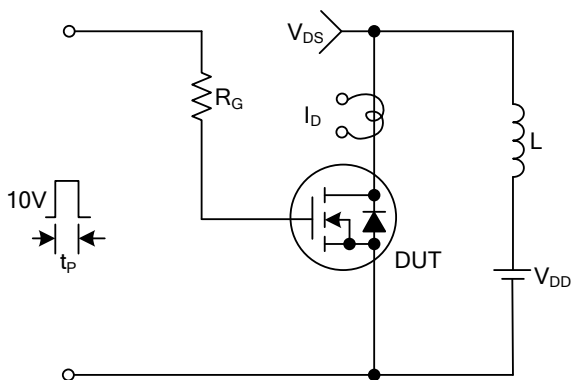
Gate Charge Waveforms



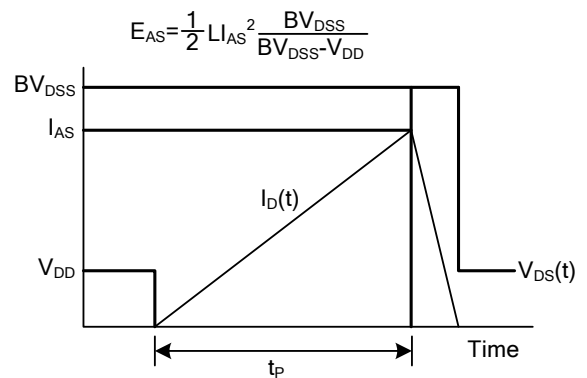
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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