



2N50K-TA

Preliminary

Power MOSFET

2A, 500V N-CHANNEL POWER MOSFET

DESCRIPTION

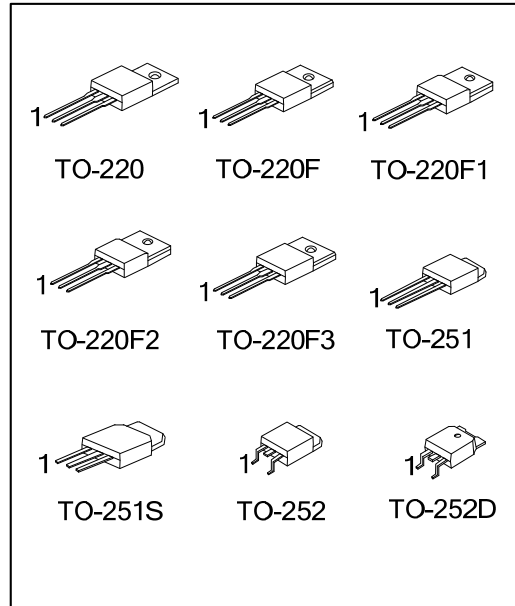
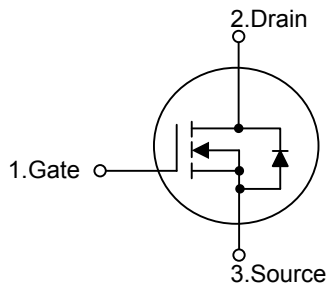
The UTC **2N50K-TA** is an N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology allows a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **2N50K-TA** is generally applied in high efficiency switch mode power supplies, active power factor correction and electronic lamp ballasts based on half bridge topology.

FEATURES

- * $R_{DS(ON)} < 4.9\Omega$ @ $V_{GS}=10V, I_D=1A$
- * High Switching Speed
- * 100% Avalanche Tested

SYMBOL



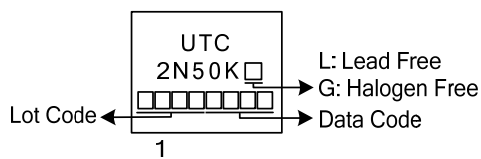
ORDERING INFORMATION

| Ordering Number | | Package | Pin Assignment | | | Packing |
|-----------------|---------------|----------|----------------|---|---|-----------|
| Lead Free | Halogen Free | | 1 | 2 | 3 | |
| 2N50KL-TA3-T | 2N50KG-TA3-T | TO-220 | G | D | S | Tube |
| 2N50KL-TF3-T | 2N50KG-TF3-T | TO-220F | G | D | S | Tube |
| 2N50KL-TF1-T | 2N50KG-TF1-T | TO-220F1 | G | D | S | Tube |
| 2N50KL-TF2-T | 2N50KG-TF2-T | TO-220F2 | G | D | S | Tube |
| 2N50KL-TF3T-T | 2N50KG-TF3T-T | TO-220F3 | G | D | S | Tube |
| 2N50KL-TM3-T | 2N50KG-TM3-T | TO-251 | G | D | S | Tube |
| 2N50KL-TMS-T | 2N50KG-TMS-T | TO-251S | G | D | S | Tube |
| 2N50KL-TN3-R | 2N50KG-TN3-R | TO-252 | G | D | S | Tape Reel |
| 2N50KL-TND-R | 2N50KG-TND-R | TO-252D | G | D | S | Tape Reel |

Note: Pin Assignment: G: Gate D: Drain S: Source

| | |
|--|--|
| <p>2N50KL-TA3-T</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p> | <p>(1) T: Tube, R: Tape Reel</p> <p>(2) TA3: TO-220, TF3: TO-220F, TF1: TO-220F1, TF2: TO-220F2, TF3T: TO-220F3, TM3: TO-251, TMS: TO-251S, TN3: TO-252, TND: TO-252D</p> <p>(3) L: Lead Free, G: Halogen Free and Lead Free</p> |
|--|--|

MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

| PARAMETER | | SYMBOL | RATINGS | UNIT |
|--|---------------------------------------|-----------|---------------------|------------------|
| Drain-Source Voltage | | V_{DSS} | 500 | V |
| Gate-Source Voltage | | V_{GSS} | ± 30 | V |
| Drain Current | Continuous ($T_C=25^\circ\text{C}$) | I_D | 2 (Note 3) | A |
| | Pulsed (Note 2) | I_{DM} | 8 (Note 3) | A |
| Avalanche Current (Note 2) | | I_{AR} | 2 | A |
| Avalanche Energy | Single Pulsed | E_{AS} | 82 | mJ |
| | Repetitive (Note 4) | E_{AR} | 3.3 | mJ |
| Power Dissipation ($T_C=25^\circ\text{C}$) | TO-220 | P_D | 52 | W |
| | TO-220F/TO-220F1 TO-220F3 | | 23 | |
| | TO-220F2 | | 23.2 | |
| | TO-251/TO-251S TO-252/TO-252D | | 50 | |
| | Derate above 25°C | | | |
| Derate above 25°C | TO-220 | 0.43 | W/ $^\circ\text{C}$ | |
| | TO-220F/TO-220F1 TO-220F3 | 0.18 | | |
| | TO-220F2 | 0.185 | | |
| | TO-251/TO-251S TO-252/TO-252D | 0.4 | | |
| | Junction Temperature | T_J | | +150 |
| Storage Temperature | | T_{STG} | -55~+150 | $^\circ\text{C}$ |

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature
3. Drain current limited by maximum junction temperature
4. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
5. $L=41\text{mH}$, $I_{AS}=2.0\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\ \Omega$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

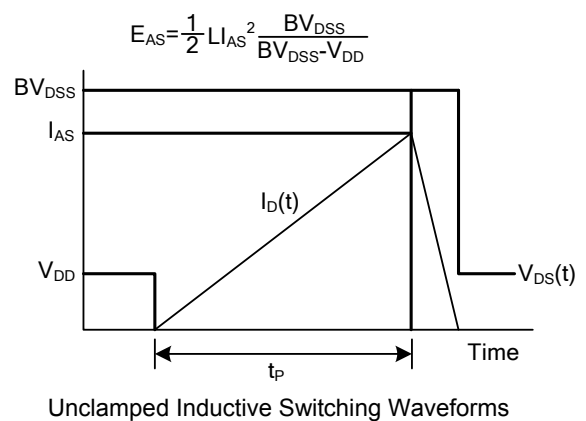
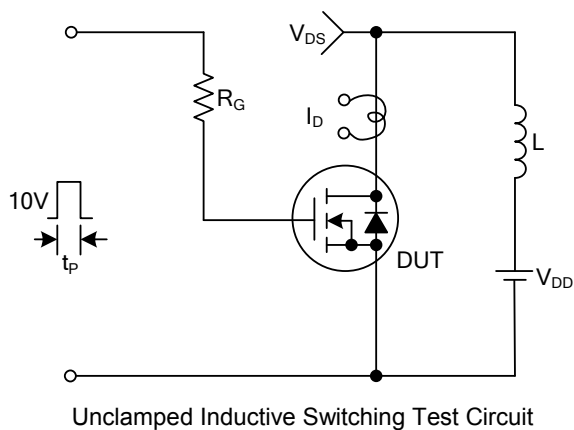
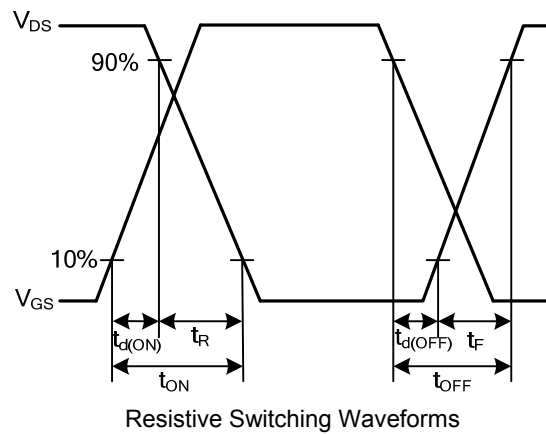
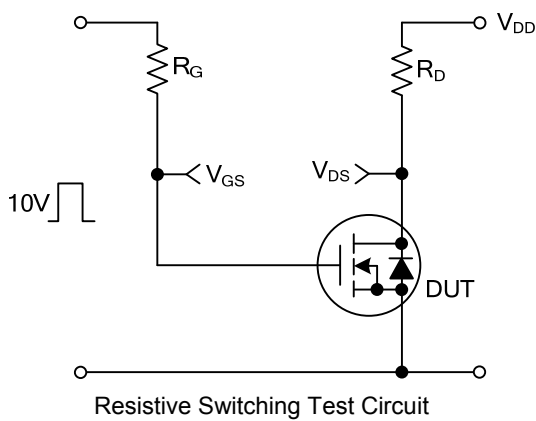
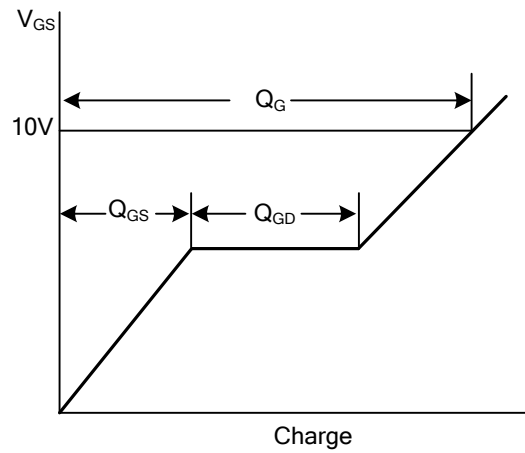
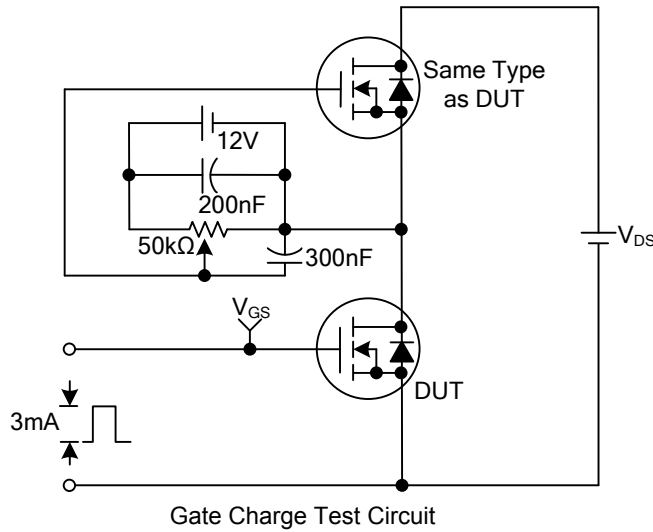
| PARAMETER | | SYMBOL | RATINGS | UNIT |
|---------------------|---|---------------|---------|--------------------|
| Junction to Ambient | TO-220/TO-220F TO-220F1/TO-220F2 TO-220F3 | θ_{JA} | 62.5 | $^\circ\text{C/W}$ |
| | TO-251/TO-251S TO-252/TO-252D | | 110 | |
| Junction to Case | TO-220 | θ_{JC} | 2.36 | $^\circ\text{C/W}$ |
| | TO-220F/TO-220F1 TO-220F3 | | 5.5 | |
| | TO-220F2 | | 5.4 | |
| | TO-251/TO-251S TO-252/TO-252D | | 2.5 | |
| | | | | |

■ ELECTRICAL CHARACTERISTICS ($T_c=25^\circ\text{C}$, unless otherwise noted)

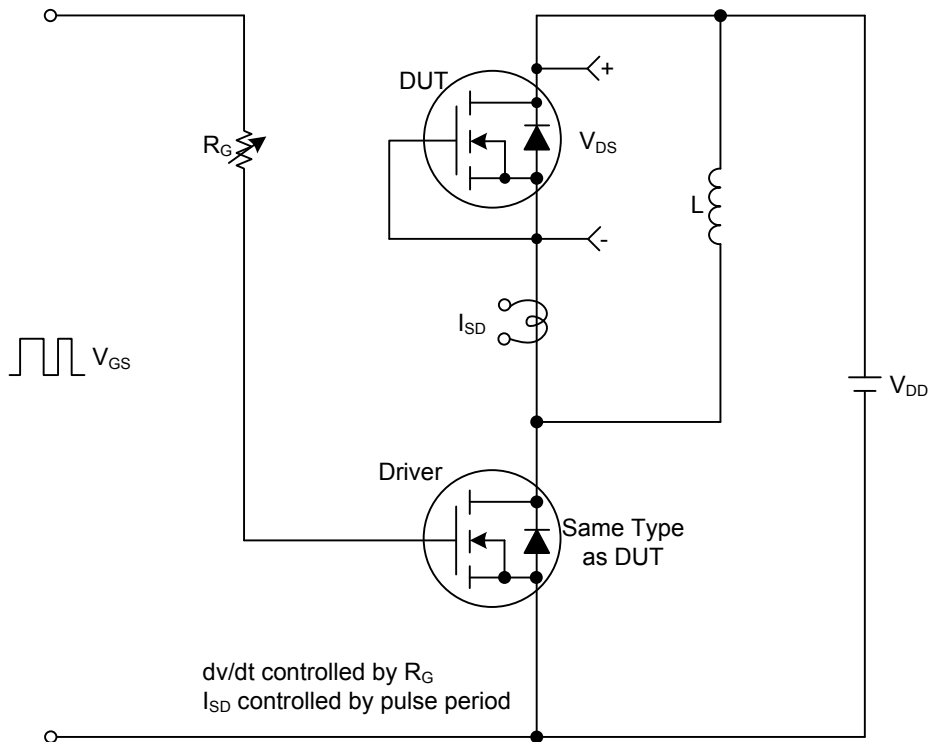
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--------------|---|-----|-----|------|---------------|
| OFF CHARACTERISTICS | | | | | | |
| Drain-Source Breakdown Voltage | BV_{DSS} | $I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$ | 500 | | | V |
| Drain-Source Leakage Current | I_{DSS} | $V_{DS}=500\text{V}$, $V_{GS}=0\text{V}$ | | | 25 | μA |
| Gate- Source Leakage Current | Forward | I_{GSS} | | | +100 | nA |
| | Reverse | | | | -100 | nA |
| ON CHARACTERISTICS | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$ | 3.0 | | 5.0 | V |
| Static Drain-Source On-State Resistance | $R_{DS(ON)}$ | $V_{GS}=10\text{V}$, $I_D=1\text{A}$ | | 2.6 | 4.9 | Ω |
| DYNAMIC PARAMETERS | | | | | | |
| Input Capacitance | C_{ISS} | $V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$ | | 200 | | pF |
| Output Capacitance | C_{OSS} | | | 39 | | pF |
| Reverse Transfer Capacitance | C_{RSS} | | | 16 | | pF |
| SWITCHING PARAMETERS | | | | | | |
| Total Gate Charge | Q_G | $V_{GS}=10\text{V}$, $V_{DS}=400\text{V}$, $I_D=2\text{A}$ (Note 1, 2) | | 12 | 25 | nC |
| Gate to Source Charge | Q_{GS} | | | 5.6 | 3 | nC |
| Gate to Drain Charge | Q_{GD} | | | 2 | 15 | nC |
| Turn-ON Delay Time | $t_{D(ON)}$ | $V_{DD}=250\text{V}$, $I_D=2\text{A}$, $R_G=25\Omega$ (Note 1, 2) | | 20 | | ns |
| Rise Time | t_R | | | 40 | | ns |
| Turn-OFF Delay Time | $t_{D(OFF)}$ | | | 84 | | ns |
| Fall-Time | t_F | | | 38 | | ns |
| SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS | | | | | | |
| Maximum Body-Diode Continuous Current | I_S | | | | 2 | A |
| Maximum Body-Diode Pulsed Current | I_{SM} | | | | 8 | A |
| Drain-Source Diode Forward Voltage | V_{SD} | $I_S=2\text{A}$, $V_{GS}=0\text{V}$ | | | 1.2 | V |

- Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
 2. Essentially independent of operating temperature

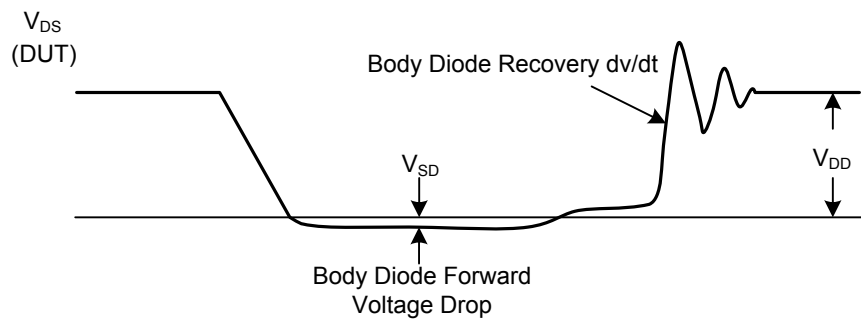
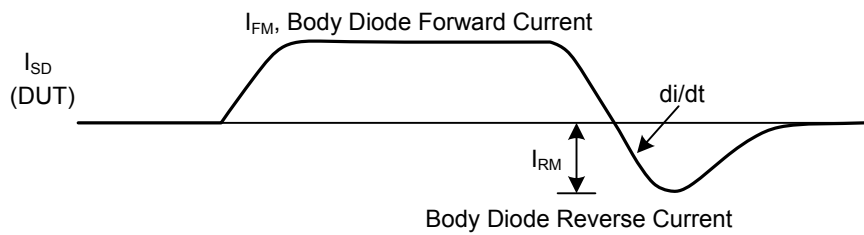
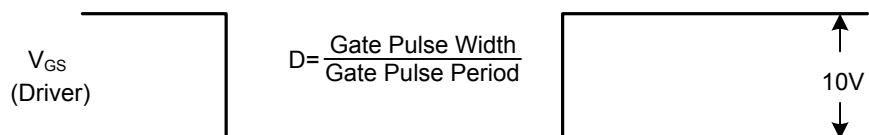
■ TEST CIRCUITS AND WAVEFORMS



■ TEST CIRCUITS AND WAVEFORMS(Cont.)



Peak Diode Recovery dv/dt Test Circuit & Waveforms



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