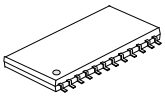
16-BIT CONSTANT CURRENT LED SINK DRIVER



SOP-24 (300 mil)

■ DESCRIPTION

The UTC **L16B45** is designed for LED displays. UTC **L16B45** contains a serial buffer and data latches which convert serial input data into parallel output format. At UTC **L16B45** output stage, sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LEDs within a large range of V_F variations.

UTC **L16B45** provides users with great flexibility and device performance while using UTC **L16B45** in their system design for LED display applications, e.g. LED panels. Users may adjust the output current from 3mA to 45mA through an external resistor, R_{ext}, which gives users flexibility in controlling the light intensity of LEDs. UTC **L16B45** guarantees to endure maximum 17V at the output port. The high clock frequency, 25MHz, also satisfies the system requirements of high volume data transmission.

■ FEATURES

* 16 constant-current output channels
* Constant output current invariant to load voltage change:
  Constant output current range:
  3~45mA @ V_{DD}=5V
  3~30mA @ V_{DD}=3.3V
* Excellent output current accuracy:
  between channels: ±3% (typ.),
  between ICs: ±6% (typ.)
* Output current adjusted through an external resistor
* Fast response of output current, $\overline{OE}$ (min.): 300ns @ V_{DD}=3.3V
* 25MHz clock frequency
* Schmitt trigger input
* 3.3V, 5V supply voltage

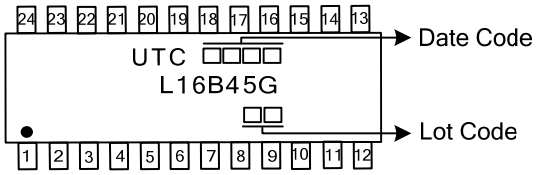
■ ORDERING INFORMATION

Ordering Number	Package	Packing
L16B45G-S24-R	SOP-24	Tape Reel

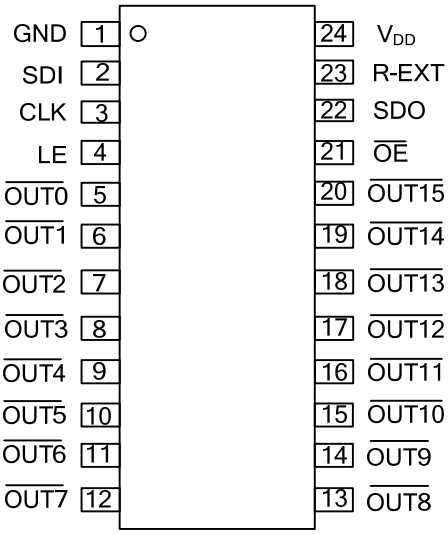
L16B45G-S24-R

(1) Packing Type	(1) R: Tape Reel
(2) Package Type	(2) S24: SOP-24
(3) Green Package	(3) G: Halogen Free and Lead Free

■ MARKING



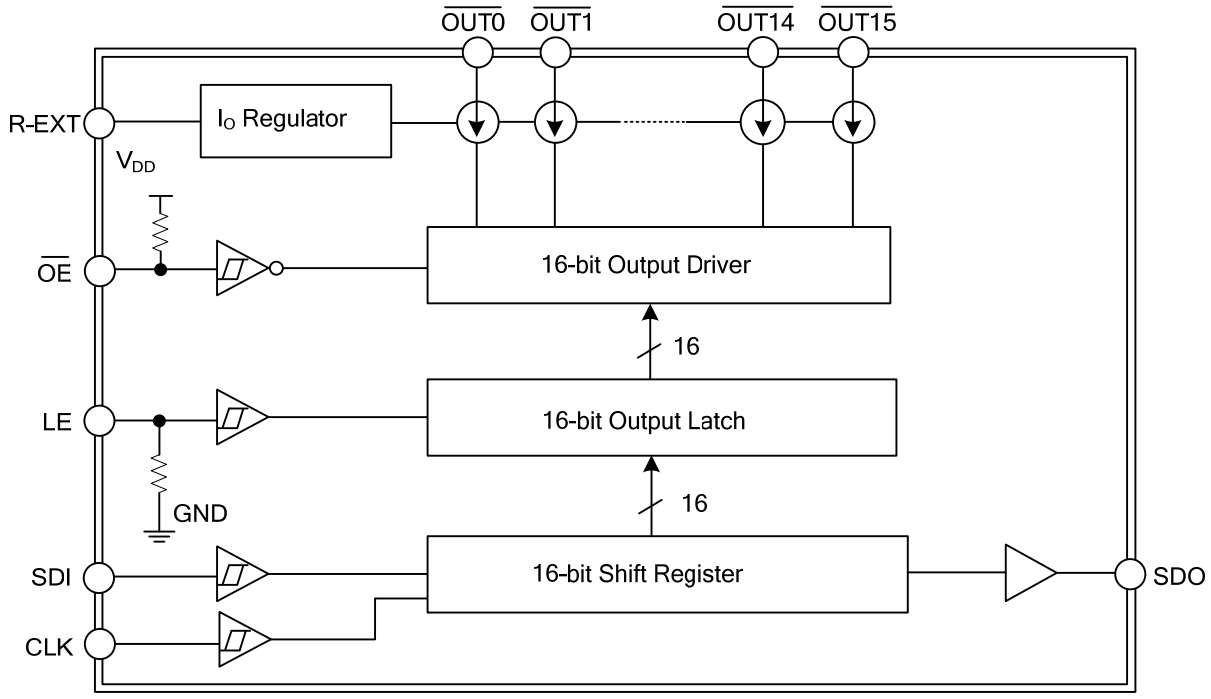
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	GND	Ground terminal for control logic and current sink
2	SDI	Serial-data input to the shift register
3	CLK	Clock input terminal for data shift on rising edge
4	LE	Data strobe input terminal Serial data is transferred to the output latch when LE is high. The data is latched when LE goes low.
5~20	$\overline{OUT0}$ ~ $\overline{OUT15}$	Constant current output terminals
21	$\overline{OE}$	Output enable terminal When (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked).
22	SDO	Serial-data output to the following SDI of next driver IC
23	R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
24	V_{DD}	3.5V/5V supply voltage terminal

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	0~7.0	V
Input Voltage	V_{IN}	-0.4~V_{DD}+0.4	V
Output Current	I_{OUT}	+90	mA
Output Voltage	V_{DS}	-0.5~+17.0	V
GND Terminal Current	I_{GND}	1000	mA
Operating Temperature	T_{OPR}	-40~+85	°C
Storage Temperature	T_{STG}	-55~+150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL RESISTANCES

PARAMETER	SYMBOL	MAX	UNIT
Junction to Ambient	θ_{JA}	70	°C/W

■ DC ELECTRICAL CHARACTERISTICS (V_{DD}=5.0V)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage		V_{DD}		4.5	5.0	5.5	V
Output Voltage		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$			17.0	V
Output Current		I_{OUT}	DC Test Circuit	3		45	mA
		I_{OH}	SDO			-1.0	mA
		I_{OL}	SDO			1.0	mA
Input Voltage	"H" Level	V_{IH}	T_A=-40~85°C	0.7×V_{DD}		V_{DD}	V
	"L" Level	V_{IL}	T_A=-40~85°C	GND		0.3×V_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V			0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA			0.4	V
		V_{OH}	I_{OH}=-1.0mA	4.6			V
Output Current 1		I_{OUT1}	V_{DS}=1.0V, R_{EXT}=1240Ω		15		mA
Current Skew		dI_{OUT1}	I_{OL}=15mA, V_{DS}=1.0V, R_{EXT}=1240Ω		±3		%
Output Current 2		I_{OUT2}	V_{DS}=1.0V, R_{EXT}=620Ω		30		mA
Current Skew		dI_{OUT2}	I_{OL}=30mA, V_{DS}=1.0V, R_{EXT}=620Ω		±3		%
Output Current vs. Output Voltage Regulation		%/dV_{DS}	V_{DS}=1.0~3.0V		±0.1		%/V
Output Current vs. Supply Voltage Regulation		%/dV_{DD}	V_{DD}=4.5~5.5V		±1.0		%/V
Pull-Up Resistor		R_{IN}(up)	$\overline{OE}$	250	500	800	KΩ
Pull-Down Resistor		R_{IN}(down)	LE	250	500	800	KΩ
Supply Current	"OFF"	I_{DD}(off) 1	R_{EXT}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		2	2.8	mA
		I_{DD}(off) 2	R_{EXT}=1240Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		4	4.8	mA
		I_{DD}(off) 3	R_{EXT}=620Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		6	6.8	mA
	"ON"	I_{DD}(on) 1	R_{EXT}=1240Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		5.2	8.2	mA
		I_{DD}(on) 2	R_{EXT}=620Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		6.5	9.5	mA

■ DC ELECTRICAL CHARACTERISTICS (V_{DD}=3.3V)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage		V_{DD}		3.0	3.3	4.5	V
Output Voltage		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$			17.0	V
Output Current		I_{OUT}	DC Test Circuit	3		30	mA
		I_{OH}	SDO			-1.0	mA
		I_{OL}	SDO			1.0	mA
Input Voltage	"H" Level	V_{IH}	T_A=-40~85°C	0.7×V_{DD}		V_{DD}	V
	"L" Level	V_{IL}	T_A=-40~85°C	GND		0.3×V_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V			0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA			0.4	V
		V_{OH}	I_{OH}=-1.0mA	2.9			V
Output Current 1		I_{OUT1}	V_{DS}=1.0V, R_{EXT}=1860Ω		10		mA
Current Skew		dI_{OUT1}	I_{OL}=10mA, V_{DS}=1.0V, R_{EXT}=1860Ω		±3		%
Output Current 2		I_{OUT2}	V_{DS}=1.0V, R_{EXT}=744Ω		25		mA
Current Skew		dI_{OUT2}	I_{OL}=25mA, V_{DS}=1.0V, R_{EXT}=744Ω		±3		%
Output Current vs. Output Voltage Regulation		%/dV_{DS}	V_{DS}=1.0~3.0V		±0.1		%/V
Output Current vs. Supply Voltage Regulation		%/dV_{DD}	V_{DD}=3.0~3.6V		±1.0		%/V
Pull-Up Resistor		R_{IN}(up)	$\overline{OE}$	250	500	800	KΩ
Pull-Down Resistor		R_{IN}(down)	LE	250	500	800	KΩ
Supply Current	"OFF"	I_{DD}(off) 1	R_{EXT}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		1.7	2.3	mA
		I_{DD}(off) 2	R_{EXT}=1860Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		3.9	4.5	mA
		I_{DD}(off) 3	R_{EXT}=744Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		5.2	5.8	mA
	"ON"	I_{DD}(on) 1	R_{EXT}=1860Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		3.9	6.0	mA
		I_{DD}(on) 2	R_{EXT}=744Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		5.2	6.5	mA

■ SWITCHING ELECTRICAL CHARACTERISTICS (V_{DD}=5.0V)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time ("L" to "H")	CLK- $\overline{OUTn}$	t_{pLH1}	V_{DD}=5.0V, V_{DS}=1.0V, V_{IH}=V_{DD}, V_{IL}=GND, R_{ext}=930Ω, V_L=4.5V, R_L=162Ω, C_L=10pF		80	100	ns
	LE- $\overline{OUTn}$	t_{pLH2}			80	100	ns
	$\overline{OE}$ - $\overline{OUTn}$	t_{pLH3}			115	135	ns
	CLK-SDO	t_{pLH}			20	40	ns
Propagation Delay Time ("H" to "L")	CLK- $\overline{OUTn}$	t_{pHL1}			80	100	ns
	LE- $\overline{OUTn}$	t_{pHL2}			80	100	ns
	$\overline{OE}$ - $\overline{OUTn}$	t_{pHL3}			115	135	ns
	CLK-SDO	t_{pHL}			20	40	ns
Pulse Width	CLK	$t_{w(CLK)}$		20			ns
	LE	$t_{w(L)}$		20			ns
	$\overline{OE}$	$t_{w(OE)}$		250			ns
Hold Time for LE		$t_{h(L)}$		5			ns
Setup Time for LE		$t_{su(L)}$		5			ns
Maximum CLK Rise Time		t_r				500	ns
Maximum CLK Fall Time		t_f				500	ns
Output Rise Time of I_{OUT}		t_{or}			160	180	ns
Output Fall Time of I_{OUT}		t_{of}			70	90	ns

■ SWITCHING ELECTRICAL CHARACTERISTICS (V_{DD}=3.3V)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time (“L” to “H”)	CLK- $\overline{OUTn}$	t_{pLH1}	V_{DD}=3.3V, V_{DS}=1.0V, V_{IH}=V_{DD}, V_{IL}=GND R_{ext}=930Ω, V_L=3.0V, R_L=100Ω, C_L=10pF		80	100	ns
	LE- $\overline{OUTn}$	t_{pLH2}			80	100	ns
	$\overline{OE}$ - $\overline{OUTn}$	t_{pLH3}			115	135	ns
	CLK-SDO	t_{pLH}			20	40	ns
Propagation Delay Time (“H” to “L”)	CLK- $\overline{OUTn}$	t_{pHL1}			100	120	ns
	LE- $\overline{OUTn}$	t_{pHL2}			80	100	ns
	$\overline{OE}$ - $\overline{OUTn}$	t_{pHL3}			115	135	ns
	CLK-SDO	t_{pHL}			20	40	ns
Pulse Width	CLK	$t_{w(CLK)}$		20			ns
	LE	$t_{w(L)}$		20			ns
	$\overline{OE}$	$t_{w(OE)}$		300	100		ns
Hold Time for LE		$t_{h(L)}$		5			ns
Setup Time for LE		$t_{su(L)}$		5			ns
Maximum CLK Rise Time		t_r				500	ns
Maximum CLK Fall Time		t_f				500	ns
Output Rise Time of I_{OUT}		t_{or}			160	180	ns
Output Fall Time of I_{OUT}		t_{of}			70	90	ns

■ APPLICATION INFORMATION

Constant Current

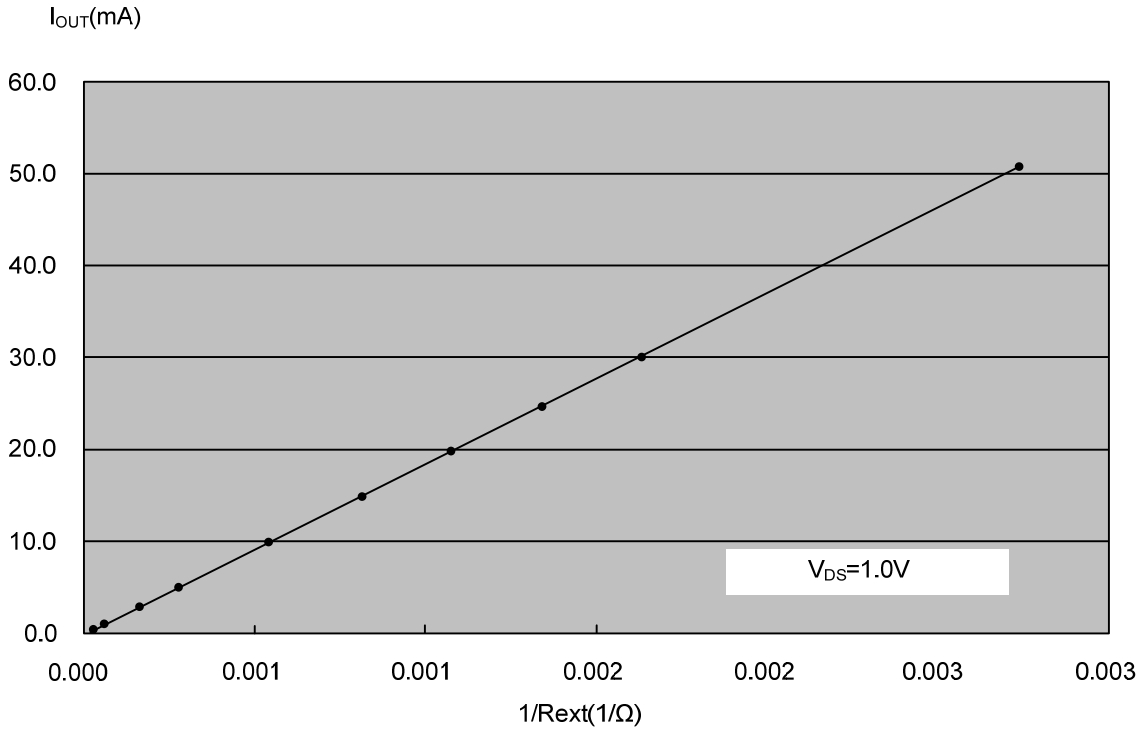
To design LED displays, UTC **L16B45** provides nearly no variations in current from channel to channel and from IC to IC. This can be achieved by:

1) The maximum current variation between channels is less than ±2.5%, and that between ICs is less than ±3%.

2) In addition, the current characteristic of output stage is flat and users can refer to the figure as shown below. The output current can be kept constant regardless of the variations of LED forward voltages (Vf). This performs as a perfection of load regulation.

Adjusting Output Current

The output current of each channel (I_{OUT}) is set by an external resistor, R_{ext}. The relationship between I_{OUT} and R_{ext} is shown in the following figure.



Also, the output current can be calculated from the equation:

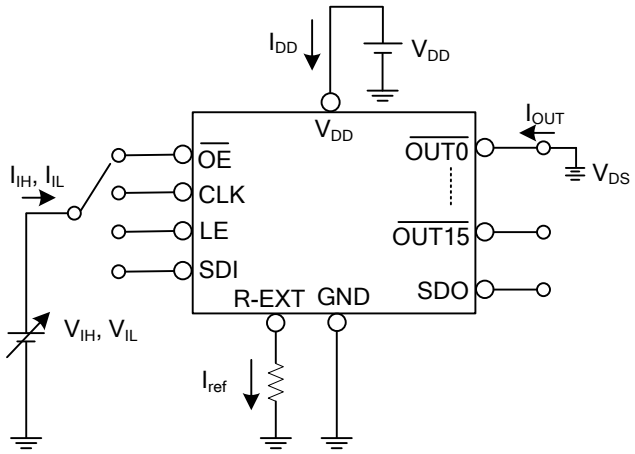
$V_{R\text{-}EXT}$=1.24V;

$I_{OUT}=V_{R\text{-}EXT}\times(1/Rext)\times15$;

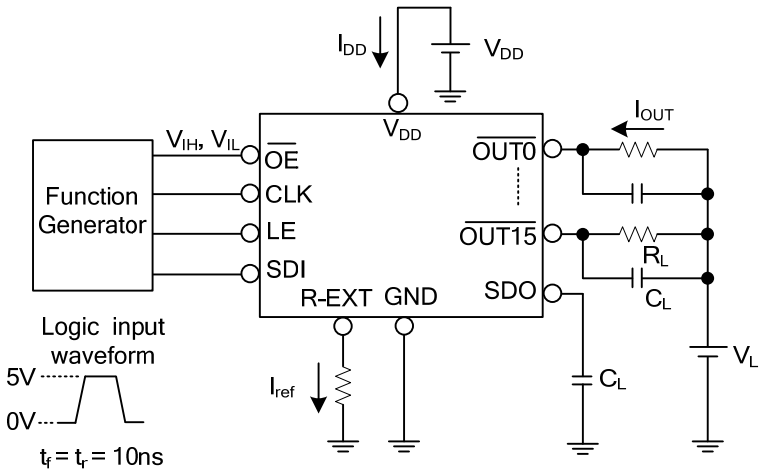
$R_{ext}=(V_{R\text{-}EXT}/I_{OUT})\times15$

where R_{ext} is the resistance of the external resistor connected to R-EXT terminal and $V_{R\text{-}EXT}$ is the voltage of R-EXT terminal. The magnitude of current (as a function of R_{ext}) is around 25mA at 744Ω and 10mA at 1860Ω.

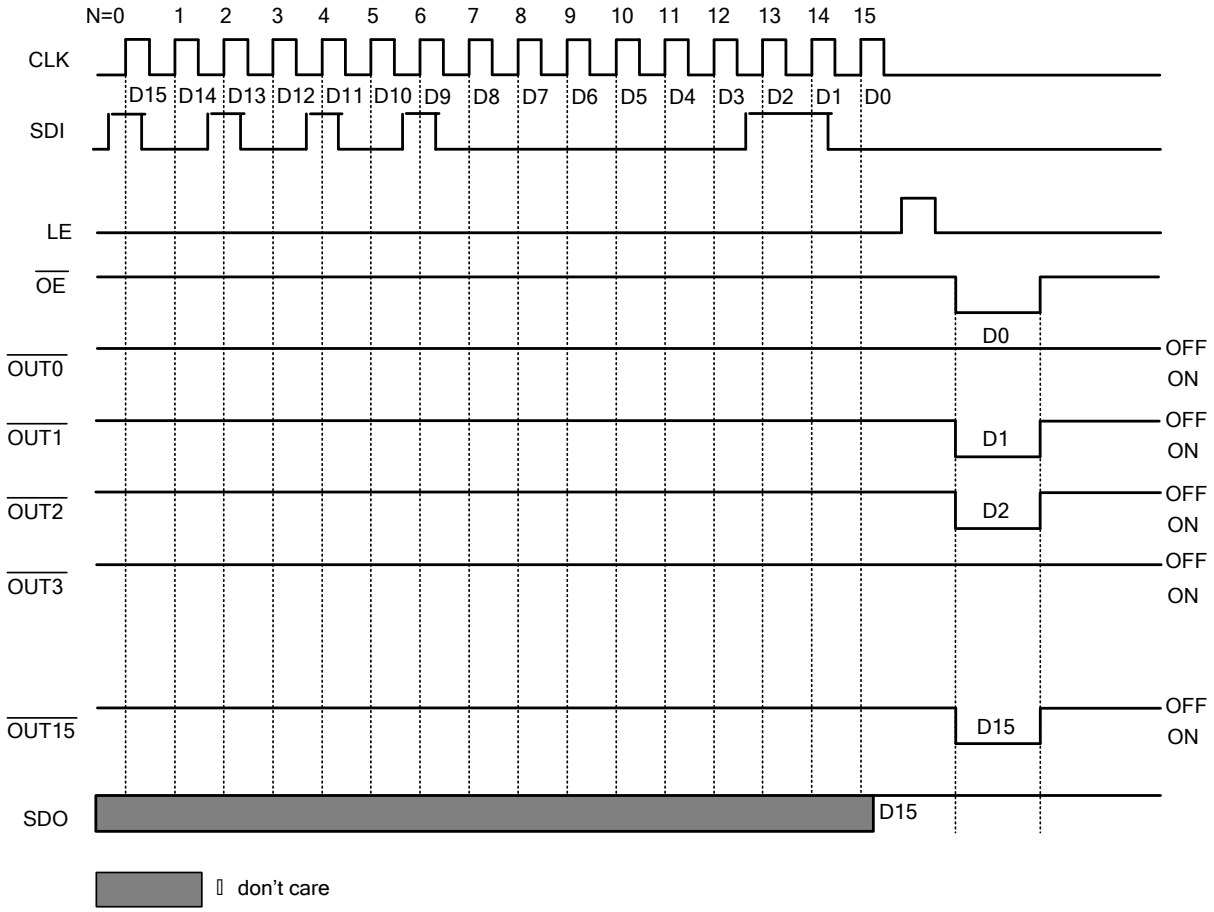
■ TEST CIRCUIT FOR DC ELECTRICAL CHARACTERISTICS



■ TEST CIRCUIT FOR SWITCHING ELECTRICAL CHARACTERISTICS



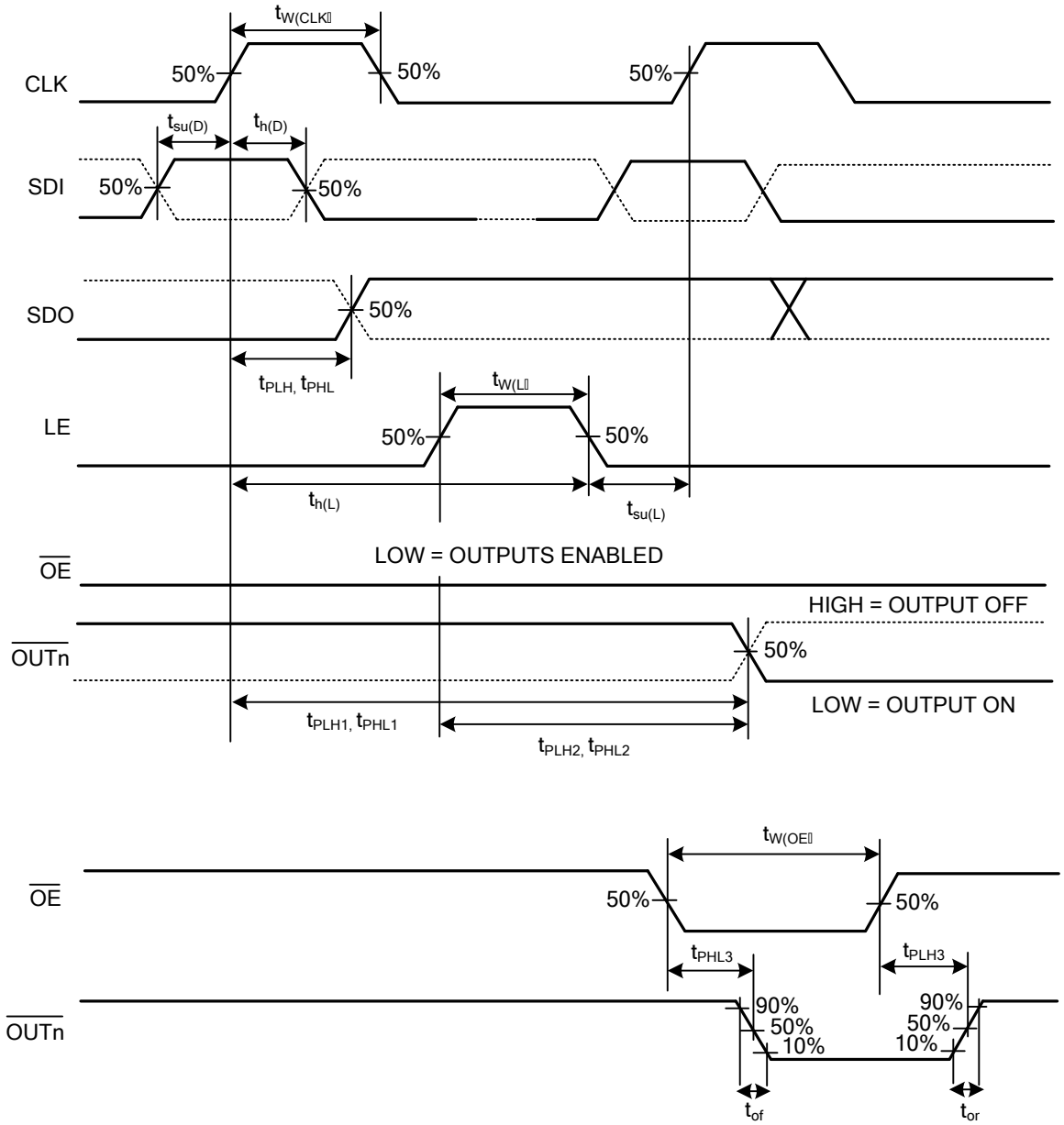
■ TIMING DIAGRAM



■ TRUTH TABLE

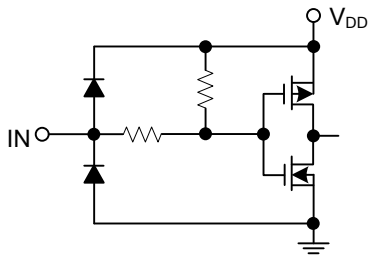
CLK	LE	$\overline{OE}$	SDI	$\overline{OUT0}$ … $\overline{OUT7}$ … $\overline{OUT15}$	SDO
↑	H	L	D_n	$\overline{D_n}$ …… $\overline{D_{n-7}}$ …. $\overline{D_{n-15}}$	D_{n-15}
↑	L	L	D_{n+1}	No Change	D_{n-14}
↑	H	L	D_{n+2}	$\overline{D_{n+2}}$ …… $\overline{D_{n-5}}$ …. $\overline{D_{n-13}}$	D_{n-13}
↓	X	L	D_{n+3}	$\overline{D_{n+2}}$ …… $\overline{D_{n-5}}$ …. $\overline{D_{n-13}}$	D_{n-13}
↓	X	H	D_{n+3}	Off	D_{n-13}

■ TIMING WAVEFORM

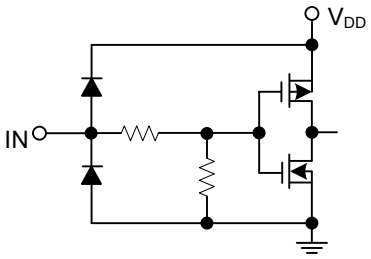


■ EQUIVALENT CIRCUITS OF INPUTS AND OUTPUTS

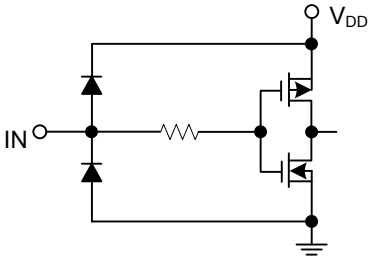
$\overline{OE}$ terminal



LE terminal



CLK, SDI terminal



SDO terminal