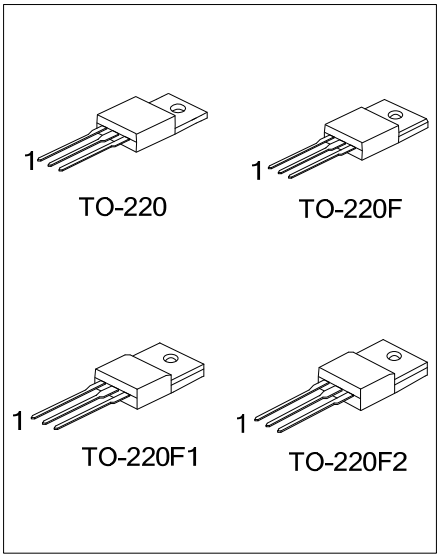
9N50K-MT

Power MOSFET

9A, 500V N-CHANNEL POWER MOSFET



■ DESCRIPTION

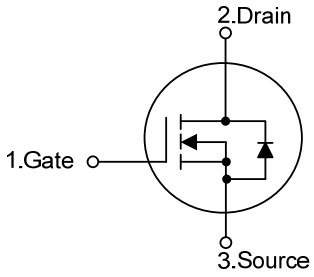
The UTC **9N50K-MT** is an N-channel mode power MOSFET using UTC's advanced technology to provide customers planar stripe and DMOS technology. This technology allows a minimum on-state resistance, superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **9N50K-MT** is generally applied in high efficiency switch mode power supplies, active power factor correction and electronic lamp ballasts based on half bridge topology.

■ FEATURES

* $R_{DS(ON)}$ < 0.85Ω @ V_{GS} = 10 V, I_D = 4.5 A
* High Switching Speed
* Improved dv/dt Capability
* 100% Avalanche Tested

■ SYMBOL



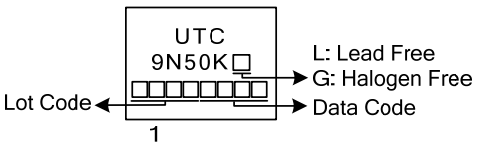
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
9N50KL-TA3-T	9N50KG-TA3-T	TO-220	G	D	S	Tube
9N50KL-TF3-T	9N50KG-TF3-T	TO-220F	G	D	S	Tube
9N50KL-TF1-T	9N50KG-TF1-T	TO-220F1	G	D	S	Tube
9N50KL-TF2-T	9N50KG-TF2-T	TO-220F2	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

9N50KL-TA3-T (1)Packing Type (2)Package Type (3)Green Package	(1) T: Tube (2) TA3: TO-220, TF3: TO-220F, TF1: TO-220F1, TF2: TO-220F2 (3) L: Lead Free, G: Halogen Free and Lead Free

■ MARKING



■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise noted)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	±30	V
Drain Current	Continuous (T_C=25°C)	I_D	9 (Note 5)	A
	Pulsed (Note 2)	I_{DM}	36 (Note 5)	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	360	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	4.5	V/ns
Power Dissipation	TO-220	P_D	140	W
	TO-220F/TO-220F1 TO-220F2		47	W
Derate above 25°C	TO-220	P_D	1.1	W/°C
	TO-220F/TO-220F1 TO-220F2		0.38	W/°C
Junction Temperature		T_J	+150	°C
Storage Temperature		T_{STG}	-55~+150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature
3. L = 8mH, I_{AS} = 9A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
4. I_{SD} ≤ 9A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
5. Drain current limited by maximum junction temperature

■ THERMAL DATA

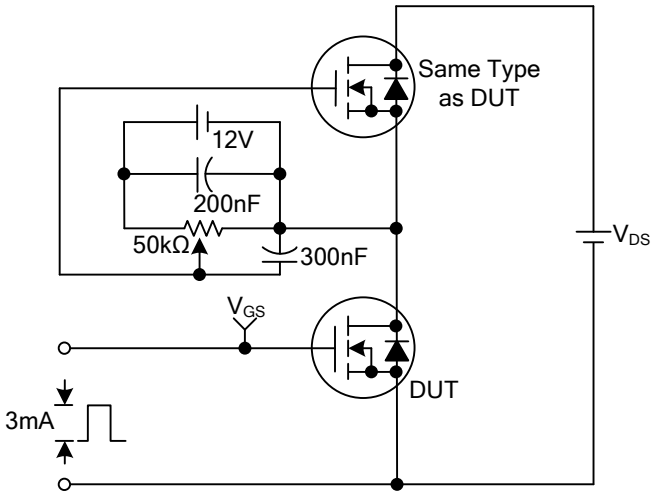
PARAMETER		SYMBOL	RATING	UNIT
Junction to Ambient		θ_{JA}	62.5	°C/W
Junction to Case	TO-220	θ_{JC}	0.8	°C/W
	TO-220F/TO-220F1 TO-220F2		2.62	°C/W

■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise noted)

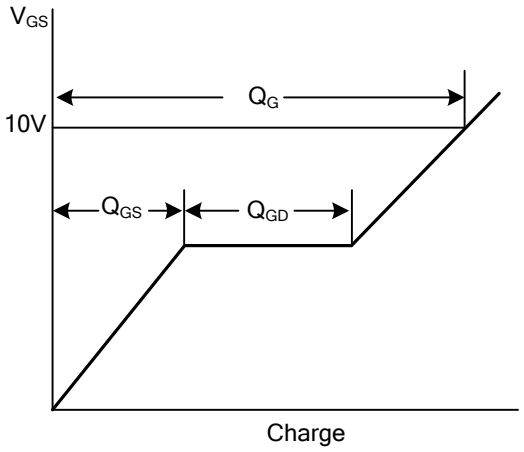
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	I_D=250μA, V_{GS}=0V	500			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=500V, V_{GS}=0V			1	μA
			V_{DS}=400V, T_C=125°C			10	
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=+30V, V_{DS}=0V			+100	nA
	Reverse		V_{GS}=-30V, V_{DS}=0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=4.5A			0.85	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	V_{GS}=0V, V_{DS}=25V, f=1.0MHz		685		pF
Output Capacitance		C_{OSS}			115		pF
Reverse Transfer Capacitance		C_{RSS}			12		pF
SWITCHING PARAMETERS							
Turn-ON Delay Time		$t_{D(ON)}$	V_{DD}=30V, I_D =0.5A, R_G =25Ω (Note 1, 2)		62		ns
Rise Time		t_R			86		ns
Turn-OFF Delay Time		$t_{D(OFF)}$			149		ns
Fall-Time		t_F			83		ns
Total Gate Charge		Q_G	V_{DS}=50V, I_D=1.3A, V_{GS}=10V (Note 1, 2)		27.2		nC
Gate to Source Charge		Q_{GS}			8.4		nC
Gate to Drain Charge		Q_{GD}			6.8		nC
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				9	A
Maximum Body-Diode Pulsed Current		I_{SM}				36	A
Drain-Source Diode Forward Voltage		V_{SD}	I_S=9A, V_{GS}=0V			1.4	V

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%
2. Essentially independent of operating temperature.

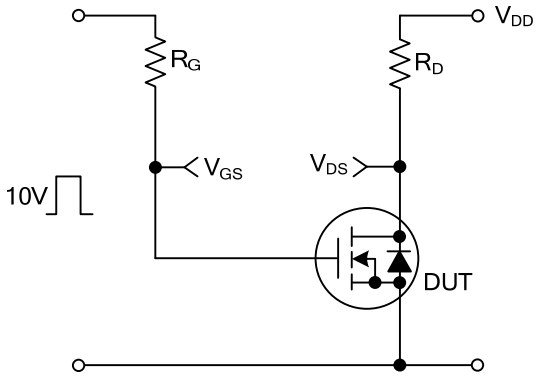
■ TEST CIRCUITS AND WAVEFORMS



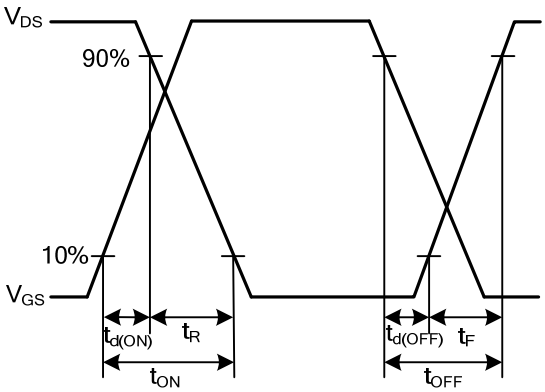
Gate Charge Test Circuit



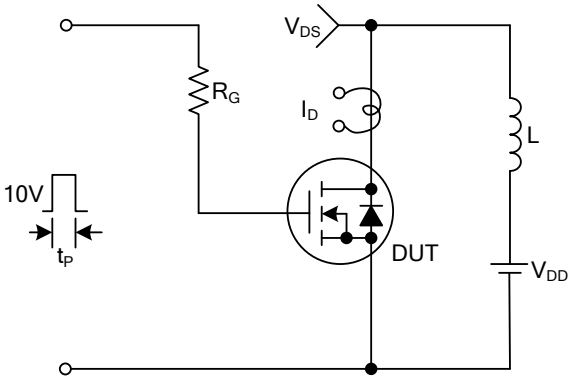
Gate Charge Waveforms



Resistive Switching Test Circuit

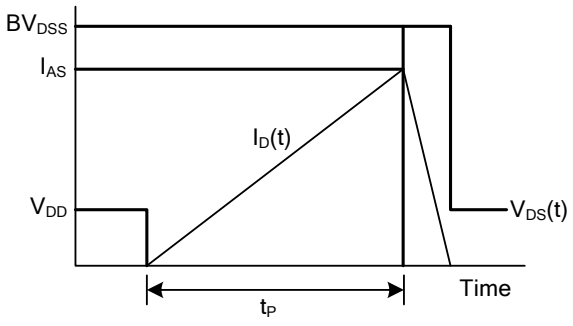


Resistive Switching Waveforms



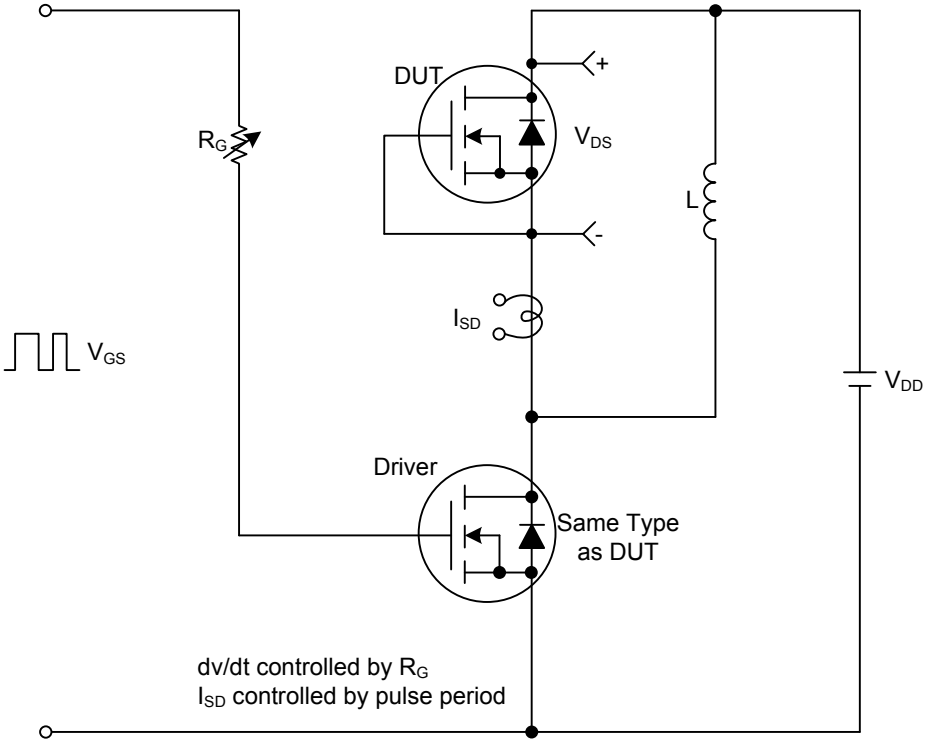
Unclamped Inductive Switching Test Circuit

$$E_{AS}=\frac{1}{2}LI_{AS}^{2}\frac{BV_{DSS}}{BV_{DSS}-V_{DD}}$$



Unclamped Inductive Switching Waveforms

■ TEST CIRCUITS AND WAVEFORMS(Cont.)



Peak Diode Recovery dv/dt Test Circuit & Waveforms