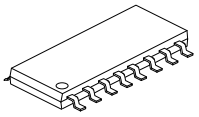
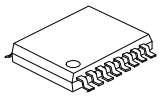
U74HC165

CMOS IC

8-BIT PARALLEL-LOAD SHIFT REGISTER



SOP-16



TSSOP-16

■ DESCRIPTION

The **U74HC165** is an 8-bit parallel-load shift register that, when clocked, shifts the data toward a serial (Q_H) output. Parallel-in access to each stage is provided by eight individual direct data (A-H) inputs that are enabled by a low level at shift/load (SH/$\overline{LD}$) input. The U74HC165 also features a clock-inhibit (CLK INH) function and a complementary serial ($\overline{Q}_H$) output.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/$\overline{LD}$ is held high and CLK INH is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH also accomplish clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. While SH/$\overline{LD}$ is low, the parallel inputs to the register are enabled independently of the levels of the CLK, CLK INH, or serial (SER) inputs.

■ FEATURES

* Complementary Outputs
* Direct Overriding Load (Data) Inputs
* Gated Clock Inputs
* Parallel-to-Serial Data Conversion

■ ORDERING INFORMATION

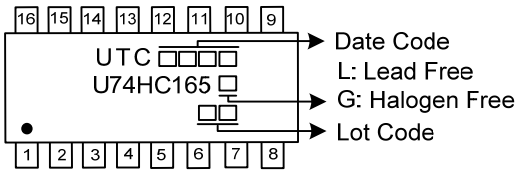
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC165L-S16-R	U74HC165G-S16-R	SOP-16	Tape Reel
U74HC165L-P16-R	U74HC165G-P16-R	TSSOP-16	Tape Reel

U74HC165G-S16-R

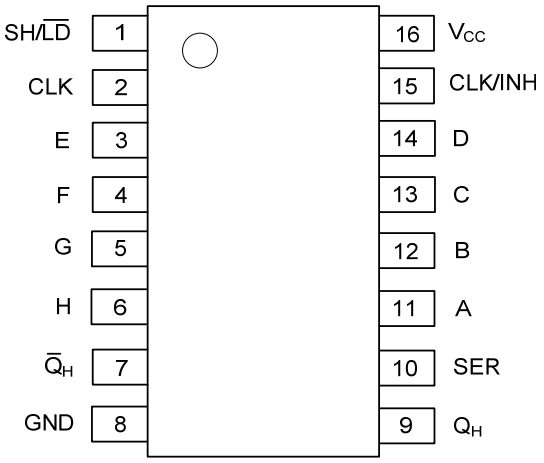
(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) S16: SOP-16, P16: TSSOP-16
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION



■ PIN DESCRIPTION

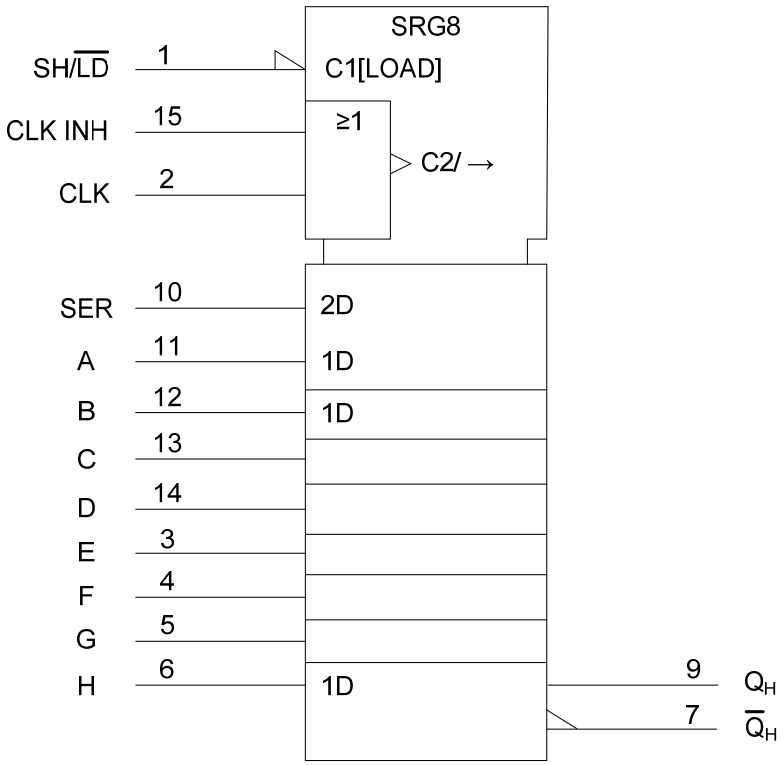
PIN NO.	PIN NAME	DESCRIPTION
1	SH/$\overline{LD}$	Asynchronous parallel load input (active LOW)
2	CLK	Clock input (LOW-to-HIGH edge-triggered)
3, 4, 5, 6 11. 12, 13, 14	A to H	Parallel data inputs (also referred to as Dn)
7	$\overline{Q}_H$	Complementary output from the last stage
8	GND	Ground (0V)
9	QH	Serial output from the last stage
10	SER	Serial data input
15	CLK/INH	Clock enable input (active LOW)
16	V_{CC}	Positive supply voltage

■ FUNCTION TABLE

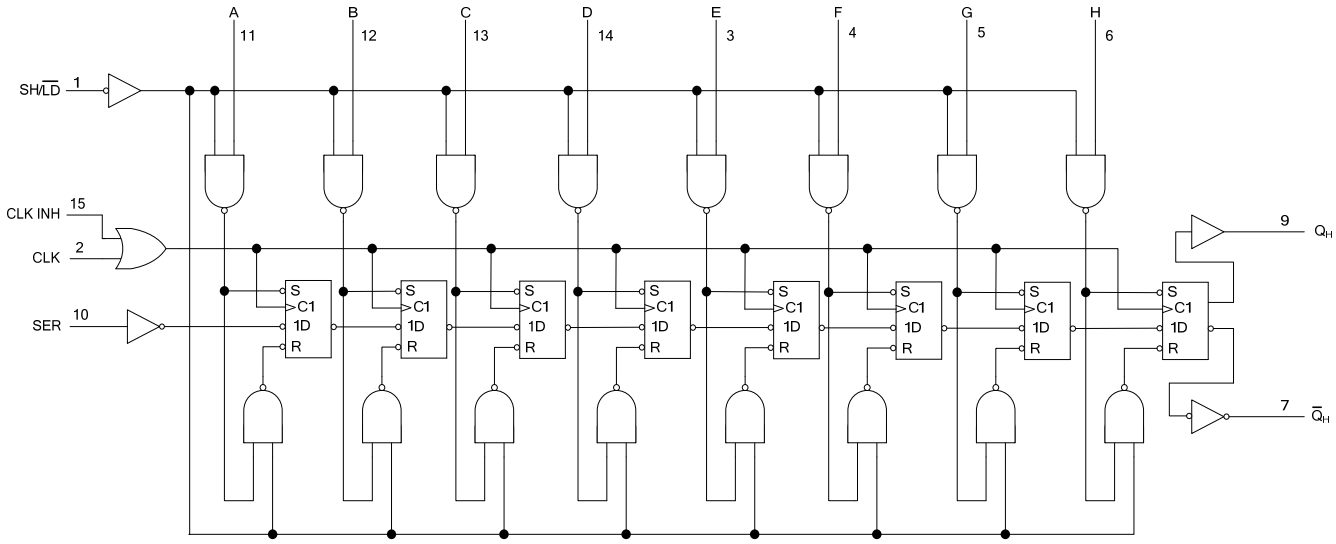
INPUTS			FUNCTION
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	No change
H	X	H	No change
H	L	↑	Shift↑
H	↑	L	Shift↑

↑ Shift=content of each internal register shifts toward serial output Q_H. Data at SER is shifted into the first register.

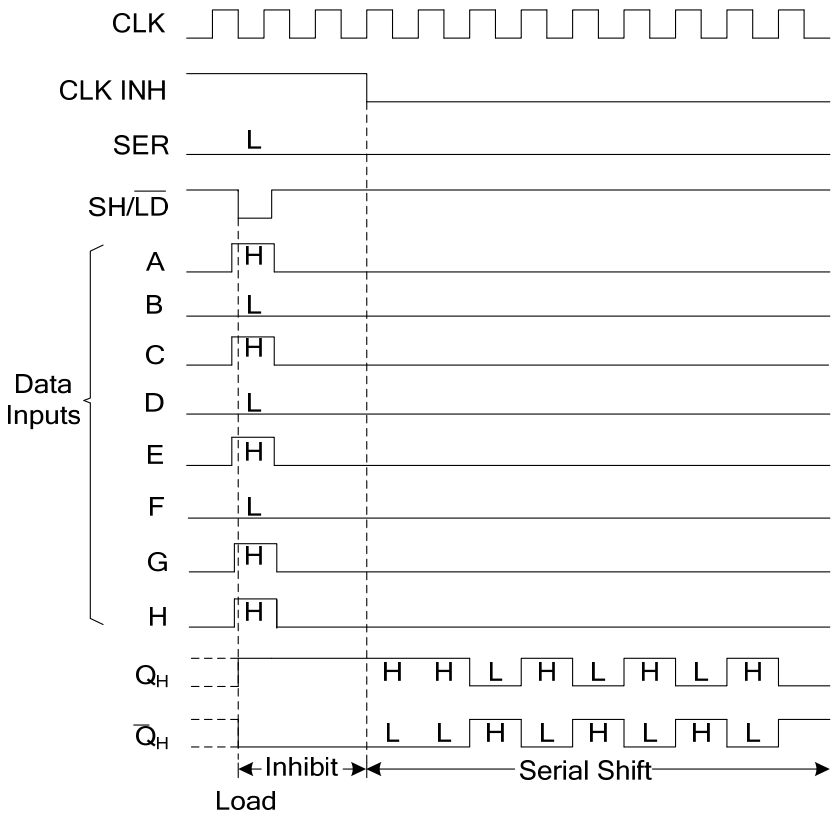
■ LOGIC SYMBOL



■ LOGIC DIAGRAM (positive logic)



■ TYPICAL SHIFT, LOAD, AND INHIBIT SEQUENCE



■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7	V
V_{CC} or GND Current	I_{CC}	±50	mA
Output Current	I_{OUT}	±25	mA
Input Clamp Current	I_{IK}	±20	mA
Output Clamp Current	I_{OK}	±20	mA
Storage Temperature	T_{STG}	-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2	5	6	V
High-level Input Voltage	V_{IH}	V_{CC}=2V	1.5			V
		V_{CC}=4.5V	3.15			V
		V_{CC}=6V	4.2			V
Low-level Input Voltage	V_{IL}	V_{CC}=2V			0.5	V
		V_{CC}=4.5V			1.35	V
		V_{CC}=6V			1.8	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition (Rise and Fall) Time	t_t	V_{CC}=2V			1000	ns
		V_{CC}=4.5V			500	ns
		V_{CC}=6V			400	ns
Operating Free-air Temperature	T_A		-40		+125	°C

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-16	θ_{JA}	73	°C/W
	TSSOP-16		110	°C/W

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A=25°C			T_A=-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage High-Level	V_{OH}	V_{CC}=2V, I_{OH}=-20μA	1.9	1.998		1.9			V
		V_{CC}=4.5V, I_{OH}=-20μA	4.4	4.499		4.4			V
		V_{CC}=6V, I_{OH}=-20μA	5.9	5.999		5.9			V
		V_{CC}=4.5V, I_{OH}=-4mA	3.98	4.3		3.7			V
		V_{CC}=6V, I_{OH}=-5.2mA	5.48	5.8		5.2			V
Output Voltage Low-Level	V_{OL}	V_{CC}=2V, I_{OL}=20μA		0.002	0.1			0.1	V
		V_{CC}=4.5V, I_{OL}=20μA		0.001	0.1			0.1	V
		V_{CC}=6V, I_{OL}=20μA		0.001	0.1			0.1	V
		V_{CC}=4.5V, I_{OL}=4mA		0.17	0.26			0.4	V
		V_{CC}=6V, I_{OL}=5.2mA		0.15	0.26			0.4	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=6V, V_{IN}= V_{CC} or GND		±0.1	±1			±1	μA
Quiescent Supply Current	I_{CC}	V_{CC}=6V, V_{IN}=V_{CC} or GND, I_{OUT}=0			8			160	μA

■ TIMING REQUIREMENTS

PARAMETER		SYMBOL	TEST CONDITIONS	T_A=25°C			T_A=-40~+125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Clock frequency		f_{clock}	V_{CC}=2V	0		6			4.2	MHz
			V_{CC}=4.5V	0		31			21	MHz
			V_{CC}=6V	0		36			25	MHz
Pulse duration	SH/$\overline{LD}$ low	t_w	V_{CC}=2V	80			120			ns
			V_{CC}=4.5V	16			24			ns
			V_{CC}=6V	14			20			ns
	CLK high or low		V_{CC}=2V	80			120			ns
			V_{CC}=4.5V	16			24			ns
			V_{CC}=6V	14			20			ns
Setup time	SH/$\overline{LD}$ high before CLK↑	t_{SU}	V_{CC}=2V	80			120			ns
			V_{CC}=4.5V	16			24			ns
			V_{CC}=6V	14			20			ns
	SER before CLK↑		V_{CC}=2V	40			60			ns
			V_{CC}=4.5V	8			12			ns
			V_{CC}=6V	7			10			ns
	CLK INH low before CLK↑		V_{CC}=2V	100			150			ns
			V_{CC}=4.5V	20			30			ns
			V_{CC}=6V	17			25			ns
	CLK INH high before CLK↑		V_{CC}=2V	40			60			ns
			V_{CC}=4.5V	8			12			ns
			V_{CC}=6V	7			10			ns
	Data before SH/$\overline{LD}$ ↓		V_{CC}=2V	100			150			ns
			V_{CC}=4.5V	20			30			ns
			V_{CC}=6V	17			25			ns
Hold time	SER data after CLK↑	t_h	V_{CC}=2V	5			5			ns
			V_{CC}=4.5V	5			5			ns
			V_{CC}=6V	5			5			ns
	PAR data after SH/$\overline{LD}$ ↓		V_{CC}=2V	5			5			ns
			V_{CC}=4.5V	5			5			ns
			V_{CC}=6V	5			5			ns

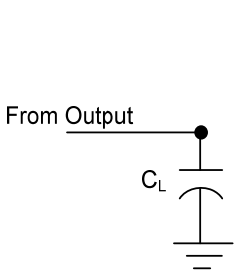
■ SWITCHING CHARACTERISTICS ($t_r = t_f = 6ns$, C_L=50Pf, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A=25°C			T_A=-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Minimum Frequency Response	f_{max}	V_{CC}=2V	6	13		4			MHz
		V_{CC}=4.5V	31	50		20			MHz
		V_{CC}=6V	36	62		24			MHz
Propagation delay from input (SH/$\overline{LD}$) to output (QH or $\overline{Q}_H$)	t_{PD}	V_{CC}=2V		80	150			250	ns
		V_{CC}=4.5V		20	30			50	ns
		V_{CC}=6V		16	26			43	ns
Propagation delay from input (CLK) to output (QH or $\overline{Q}_H$)		V_{CC}=2V		75	150			250	ns
		V_{CC}=4.5V		15	30			50	ns
		V_{CC}=6V		13	26			43	ns
Propagation delay from input (H) to output (QH or $\overline{Q}_H$)		V_{CC}=2V		75	150			180	ns
		V_{CC}=4.5V		15	30			36	ns
		V_{CC}=6V		13	26			31	ns
To Output (Any)	t_t	V_{CC}=2V		38	75			110	ns
		V_{CC}=4.5V		8	15			22	ns
		V_{CC}=6V		6	13			19	ns

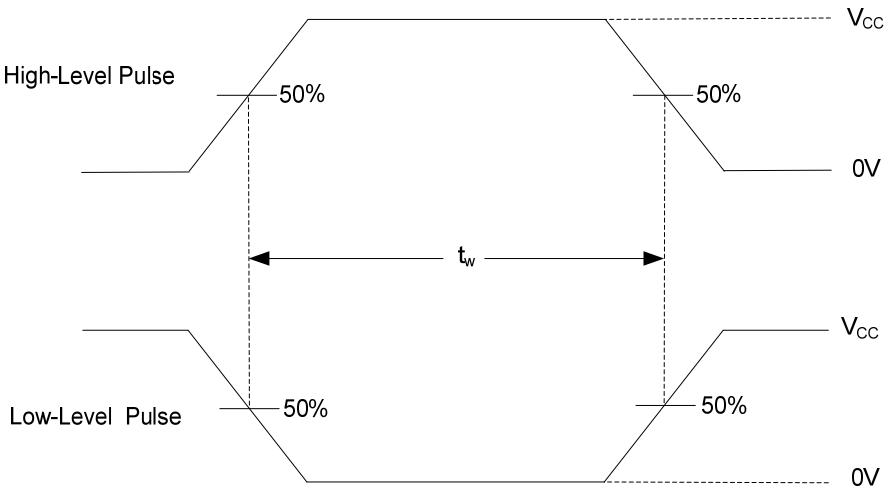
■ OPERATING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C_I	V_{CC}=2V to 6V		3	10	pF
Power Dissipation Capacitance	C_{PD}	No load		75		pF

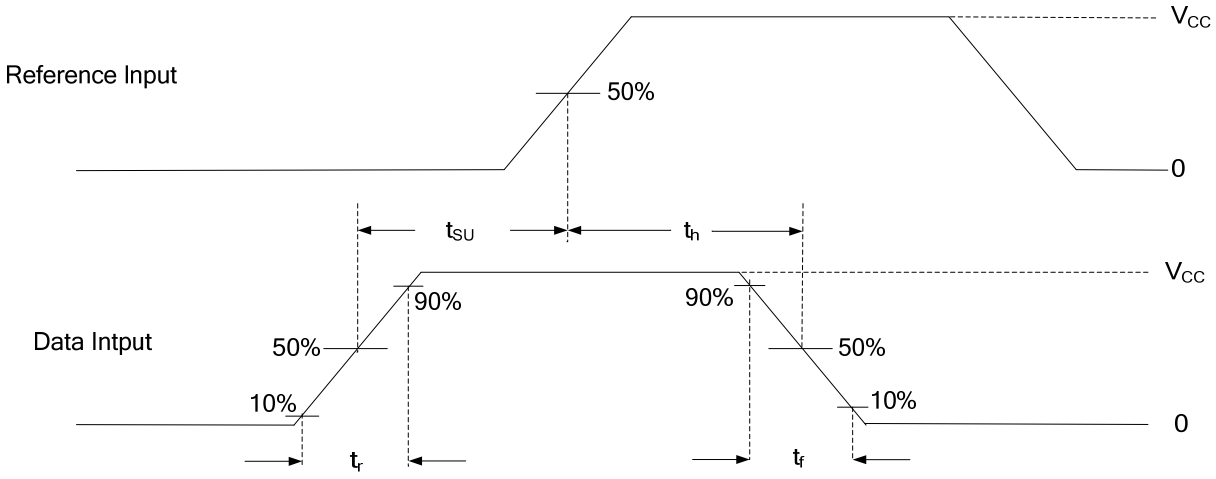
■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

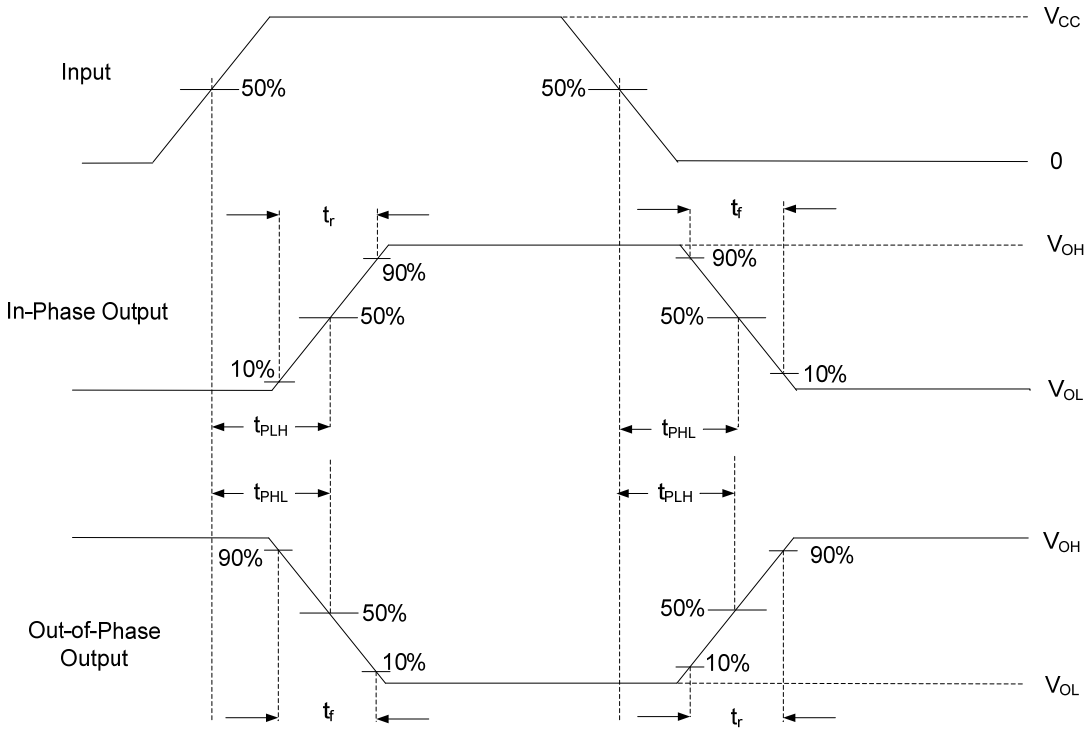


PULSE DURATIONS



SETUP AND HOLD AND INPUT RISE AND FALL TIMES

■ TEST CIRCUIT AND WAVEFORMS (Cont.)



PROPAGATION DELAY AND OUTPUT TRANSITION TIMES