UNISONIC TECHNOLOGIES CO., LTD

U74AHC595

CMOS IC

8-BIT SHIFT REGISTER WITH 3-STATE OUTPUT REGISTERS

SOP-16

SSOP-16 (150mil)

TSSOP-16

■ DESCRIPTION

The UTC **74AHC595** contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage registers. The shift register has a direct overriding clear ($\overline{\text{SRCLR}}$) input, serial (SER) input, and a serial output for cascading. When the output-enable ($\overline{\text{OE}}$) input is high, all outputs, except $Q_{H'}$, are in the high-impedance state.

Both the shift-register clock (SRCLK) and storage-register clock (RCLK) are positive-edge triggered. If both clocks are connected together the shift register always is one clock pulse ahead of the storage register.
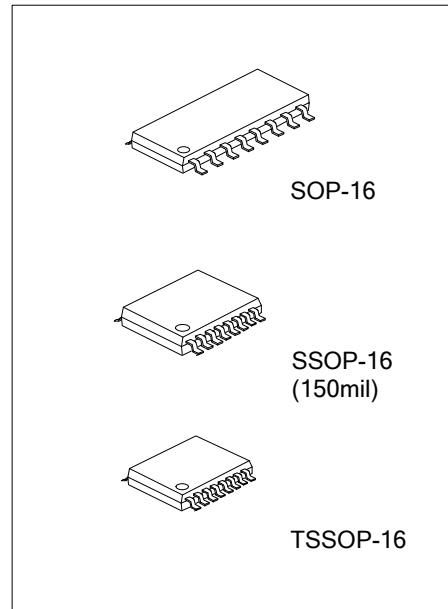
■ FEATURES

* Operation Voltage Range: 2 ~ 5.5V
* Shift Register Has Direct Clear
* 8-bit Serial-In, Parallel-Out Shift

■ ORDERING INFORMATION

| Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AHC595L-S16-R	U74AHC595G-S16-R	SOP-16	Tape Reel
U74AHC595L-R16-R	U74AHC595G-R16-R	SSOP-16	Tape Reel
U74AHC595L-P16-R	U74AHC595G-P16-R	TSSOP-16	Tape Reel

U74AHC595<u>G</u>-<u>S16</u>-<u>R</u>

(1) Packing Type
(2) Package Type
(3) Green Package

(1) R: Tape Reel

(2) S16: SOP-16, R16: SSOP-16, P16: TSSOP-16

(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING

SOP-16 / TSSOP-16	SSOP-16

UTC □□□□
U74AHC595□
→ Date Code
L: Lead Free
G: Halogen Free
Lot Code

UTC □□□□
AHC595□
→ Date Code
L: Lead Free
G: Halogen Free
Lot Code

QW-R502-997.F

■ **PIN CONFIGURATION**

QB	1	○		16	V_CC
QC	2			15	QA
QD	3			14	SER
QE	4			13	$\overline{OE}$
QF	5			12	RCLK
QG	6			11	SRCLK
QH	7			10	$\overline{SRCLR}$
GND	8			9	QH'
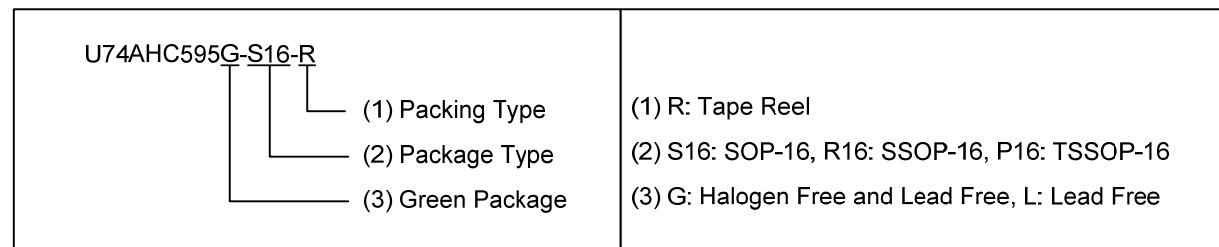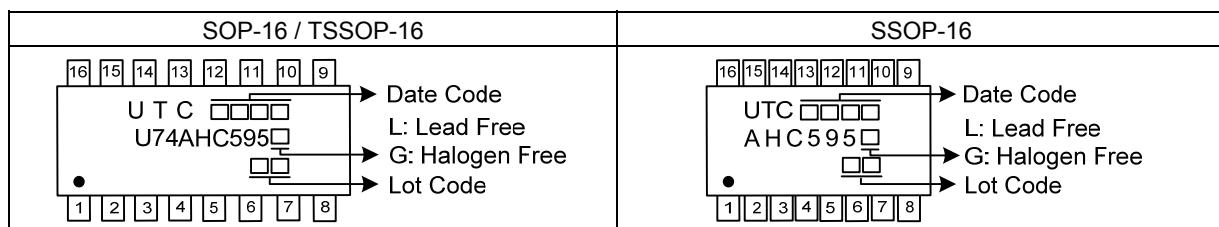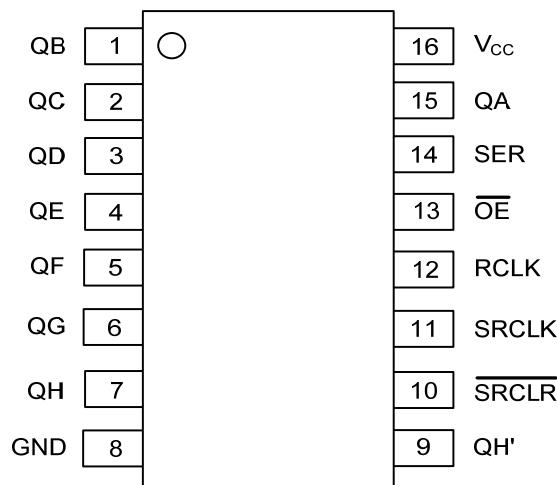
■ **FUNCTION TABLE**

FUNCTION	INPUTS					OUTPUTS	
	SRCLK	RCLK	$\overline{OE}$	$\overline{SRCLR}$	SER	QH'	Qn
A Low-Level on $\overline{SRCLR}$ only affects the shift registers.	X	X	L	L	X	L	NC
Empty shift register loaded into storage register.	X	↑	L	L	X	L	L
Shift register clear. Parallel outputs in high-impedance OFF-state	X	X	H	L	X	L	Z
Logic high level shifted into the first shift register. Contents of all shift register stages shifted through, e.g. previous state of stage G(internal QG') appears on the serial output(QH').	↑	X	L	H	H	QG'	NC
Contents of shift register stages (internal Qn') are transferred to the storage register and parallel output stages.	X	↑	L	H	X	NC	Qn'
Contents of shift register shifted through. Previous contents of the shift register is transferred to the storage register and the parallel output stages.	↑	↑	L	H	X	QG'	Qn'

Note:H : HIGH voltage level.
　　　L : LOW voltage level.
　　　X : Don't care.
　　　Z : High impedance OFF-state.
　　　NC: No change.
　　　↑ : Low-to-High transition.
　　　↓ : High-to-Low transition.

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■ **LOGIC DIAGRAM (POSITIVE LOGIC)**
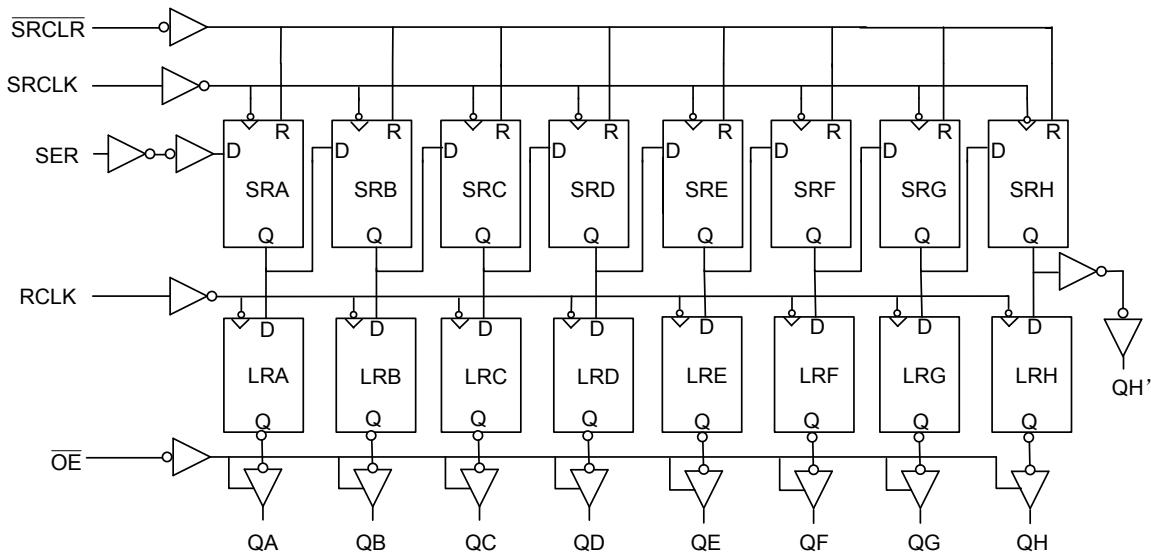
■ **TIMING DIAGRAM**
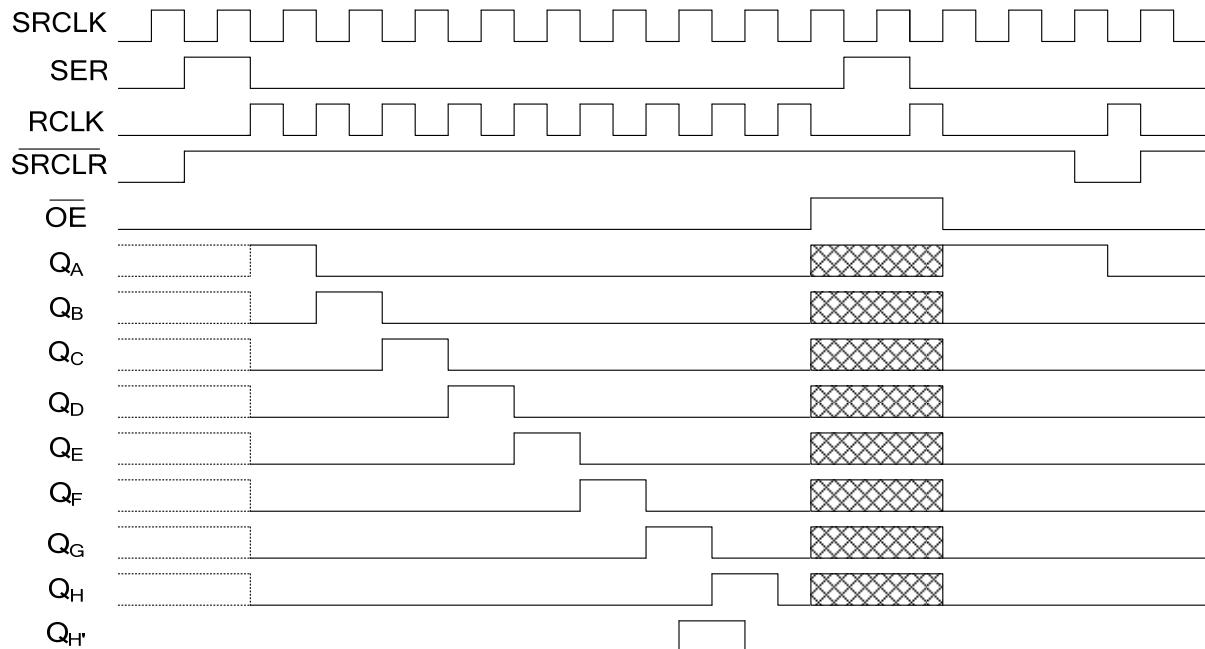
Note: ▨▨▨▨ Implies that the outputs is in 3-State mode.

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QW-R502-997.F

■ **ABSOLUTE MAXIMUM RATING** (unless otherwise specified)(Note 2)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7.0	V
Input Voltage	V_{IN}	-0.5 ~ 7.0	V
Output Voltage(active mode)	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Clamp Current (V_{iN}<0)	I_{IK}	-20	mA
Output Clamp Current (V_{OUT}<0)	I_{OK}	±20	mA
Output Current	I_{OUT}	±25	mA
V_{CC} or GND Current	I_{CC}	±75	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-16	θ_{JA}	73	°C/W
	SSOP-16		90	
	TSSOP-16		108	

■ **RECOMMENDED OPERATING CONDITIONS**

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CC}	2		5.5	V
Input Voltage		V_{IN}	0		5.5	V
Output Voltage		V_{OUT}	0		V_{CC}	V
Input Transition Rise or Fall Rate	V_{CC}=3.3±0.3V	Δt/Δv			100	ns/V
	V_{CC}=5±0.5V				20	
Operating Temperature		T_A	-40		+125	°C

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■ **ELECTRICAL CHARACTERISTICS** (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A=25°C			T_A=-40°C~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
HIGH-level input voltage	V_{IH}	V_{CC}=2V	1.5			1.5			V
		V_{CC}=3V	2.1			2.1			
		V_{CC}=5.5V	3.85			3.85			
LOW-lever output voltage	V_{IL}	V_{CC}=2V			0.5			0.5	V
		V_{CC}=3V			0.9			0.9	
		V_{CC}=5.5V			1.65			1.65	
High-Level Output Voltage	V_{OH}	V_{CC}=2V, I_{OH}=-50µA	1.9	2		1.9			V
		V_{CC}=3V, I_{OH}=-50µA	2.9	3		2.9			
		V_{CC}=4.5V, I_{OH}=-50µA	4.4	4.5		4.4			
		V_{CC}=3V, I_{OH}=-4mA	2.58			2.40			
		V_{CC}=4.5V, I_{OH}=-8mA	3.94			3.70			
Low-Level Output Voltage	V_{OL}	V_{CC}=2V, I_{OL}=50µA			0.1			0.1	V
		V_{CC}=3V, I_{OL}=50µA			0.1			0.1	
		V_{CC}=4.5V, I_{OL}=50µA			0.1			0.1	
		V_{CC}=3V, I_{OL}=4mA			0.36			0.55	
		V_{CC}=4.5V, I_{OL}=8mA			0.36			0.55	
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=0 ~ 5.5V, I_{IN}=5.5V or GND			±0.1			±2	µA
Output Off-state Current	I_{OZ}	V_{CC}=5.5V, V_{IN}=V_{CC} or GND, V_{OUT}=V_{CC} or GND, $\overline{OE}$ =V_{IH} or V_{IL}			±0.25			±10	µA
Quiescent Supply Current	I_{CC}	V_{CC}=5.5V, V_{IN}=GND or V_{CC}, I_{OUT}=0			4			80	µA

■ **DYNAMIC CHARACTERISTICS** (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A=25°C			T_A=-40°C~+125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Maximum Clock Frequency	f_{max}	V_{CC}=3.3±0.3V	C_L=15pF	80	120		50			MHz
			C_L=50pF	55	105		30			MHz
		V_{CC}=5±0.5V	C_L=15pF	135	170		90			MHz
			C_L=50pF	95	140		70			MHz
Propagation delay from input RCLK to output Q_A-Q_H	t_{PLH}	V_{CC}=3.3±0.3V	C_L=15pF		8	13			16	ns
			C_L=50pF		10	16			19	ns
		V_{CC}=5±0.5V	C_L=15pF		5	9			11	ns
			C_L=50pF		6.5	11			13	ns
	t_{PHL}	V_{CC}=3.3±0.3V	C_L=15pF		8	13			16	ns
			C_L=50pF		10	16			19	ns
		V_{CC}=5±0.5V	C_L=15pF		5	9			11	ns
			C_L=50pF		6.5	11			13	ns
Propagation delay from input SRCLK to output QH'	t_{PLH}	V_{CC}=3.3±0.3V	C_L=15pF		6.6	13			16.5	ns
			C_L=50pF		9.2	16.5			20.1	ns
		V_{CC}=5±0.5V	C_L=15pF		4.5	8.2			10.5	ns
			C_L=50pF		8	11			13	ns
	t_{PHL}	V_{CC}=3.3±0.3V	C_L=15pF		6.6	13			16.5	ns
			C_L=50pF		9.2	16.5			20.1	ns
		V_{CC}=5±0.5V	C_L=15pF		4.5	8.2			10.5	ns
			C_L=50pF		8	11			13	ns
Propagation delay from input $\overline{SRCLR}$ to output QH'	t_{PHL}	V_{CC}=3.3±0.3V	C_L=15pF		6.2	12.8			15	ns
			C_L=50pF		9	16.3			18.7	ns
		V_{CC}=5±0.5V	C_L=15pF		4.5	8			10	ns
			C_L=50pF		6.4	10			12	ns
Propagation delay from input $\overline{OE}$ to output Q_A-Q_H	t_{PZH}	V_{CC}=3.3±0.3V	C_L=15pF		6	11.5			15	ns
			C_L=50pF		7.8	15			18.5	ns
		V_{CC}=5±0.5V	C_L=15pF		4.3	8.6			11	ns
			C_L=50pF		5.7	10.6			13	ns
	t_{PZL}	V_{CC}=3.3±0.3V	C_L=15pF		7.8	11.5			15.0	ns
			C_L=50pF		9.6	15			18.5	ns
		V_{CC}=5±0.5V	C_L=15pF		5.4	8.6			11	ns
			C_L=50pF		6.8	10.6			13	ns
Propagation delay from input $\overline{OE}$ to output Q_A-Q_H	t_{PHZ}	V_{CC}=3.3±0.3V	C_L=50pF		8.1	15.7			17.5	ns
		V_{CC}=5±0.5V			3.5	10.3			12	ns
	t_{PLZ}	V_{CC}=3.3±0.3V			9.3	15.7			17.5	ns
		V_{CC}=5±0.5V			3.4	10.3			12	ns

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■ **TIMING REQUIREMENTS** (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A=25°C			T_A=-40°C~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Pulse duration, SRCLK high or low	t_W	V_{CC}=3.3±0.3V	5			5			ns
		V_{CC}=5±0.5V	5			5			ns
Pulse duration, RCLK high or low		V_{CC}=3.3±0.3V	5			5			ns
		V_{CC}=5±0.5V	5			5			ns
Pulse duration, $\overline{SRCLR}$ low		V_{CC}=3.3±0.3V	5			5			ns
		V_{CC}=5±0.5V	5			5			ns
Setup Time, SER before SRCLK↑	t_{SU}	V_{CC}=3.3±0.3V	3.5			3.5			ns
		V_{CC}=5±0.5V	3			3			ns
Setup Time, SRCLK↑ before RCLK↑		V_{CC}=3.3±0.3V	8			8			ns
		V_{CC}=5±0.5V	5			5			ns
Setup Time, $\overline{SRCLR}$ low before RCLK↑		V_{CC}=3.3±0.3V	8			8			ns
		V_{CC}=5±0.5V	5			5			ns
Setup Time, $\overline{SRCLR}$ high (inactive) before SRCLK↑		V_{CC}=3.3±0.3V	3			3			ns
		V_{CC}=5±0.5V	2.5			2.5			ns
Hold Time, SER after SRCLK↑	t_H	V_{CC}=3.3±0.3V	1.5			1.5			ns
		V_{CC}=5±0.5V	2			2			ns

■ **OPERATING CHARACTERISTICS** (V_{CC}=5V, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C_{IN}	V_{CC}=5V, V_{IN}=V_{CC} or GND		3	10	
Output Capacitance	C_{OUT}	V_{CC}=5V, V_{OUT}=V_{CC} or GND		5.5		
Power Dissipation Capacitance	C_{PD}	No load, f=1MHz		25.2		pF

■ **TEST CIRCUIT AND WAVEFORMS**
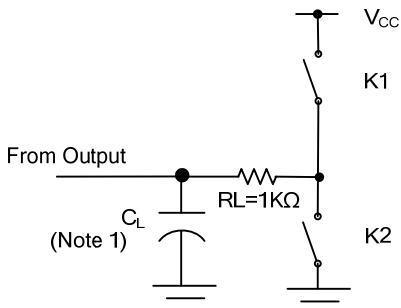
TEST	K1	K2
t_{PLH}/t_{PHL}	Open	Open
t_{PHZ}/t_{PZH}	Open	Close
t_{PLZ}/t_{PZL}	Close	Open
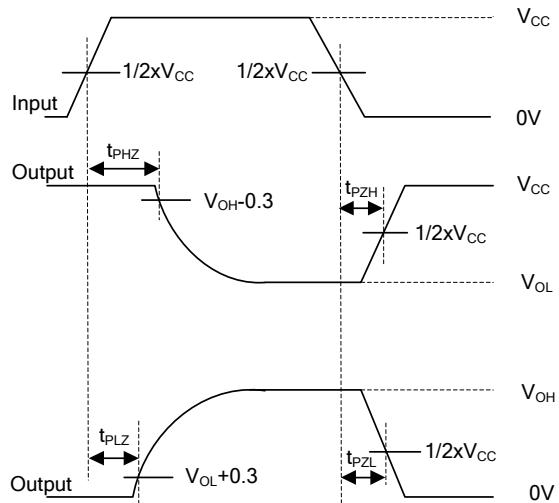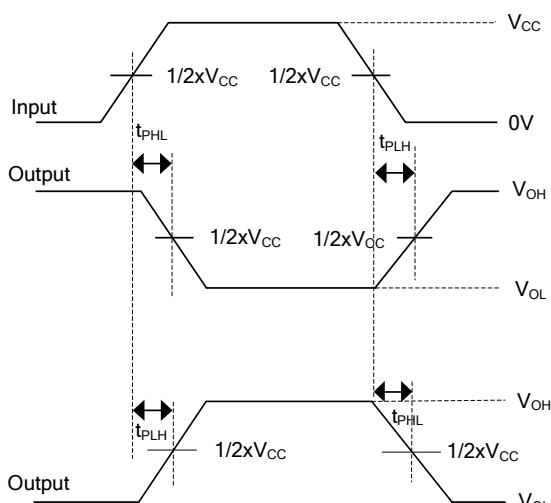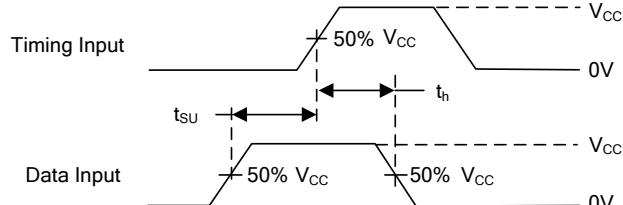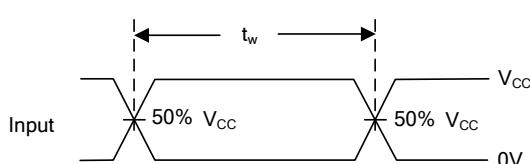
Note: 1. C_L includes probe and jig capacitance.
  2. All input pulses are supplied by generators having the following characteristics:
    PRR ≤1MHZ, Z_O=50Ω, t_r ≤3ns, t_f ≤3ns.
  3. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms